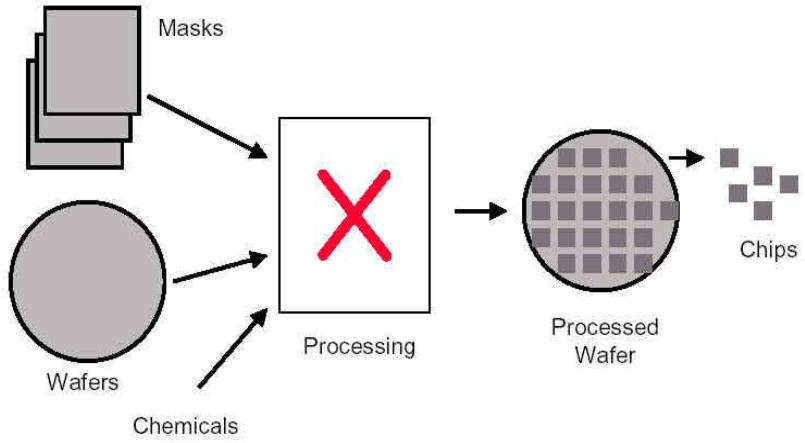
Disseny físic (layout)

Sebastià Bota

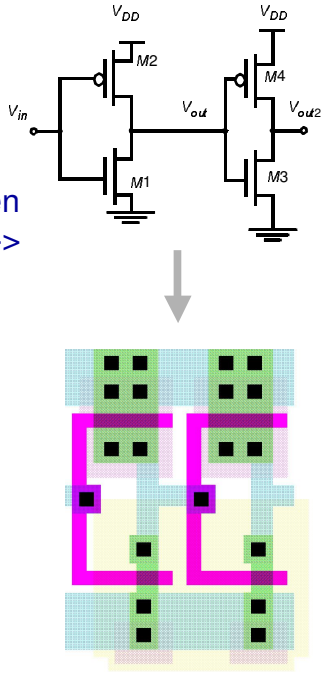
Sistemes Microelectrònics
Assignatura Optativa

Qué és necessita per fabricar un circuit integrat



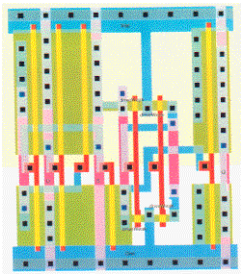
Disseny de CI: Layout

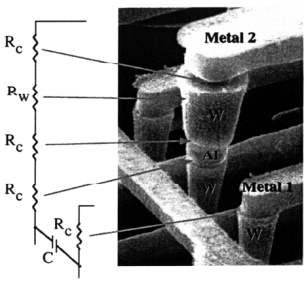
- Layout: disseny de les màscares pel procés de litografia
- Les limitacions tecnològiques impliquen restriccions a l'hora de fer el disseny >> REGLES DE DISSENY
- Dues formes i mitja de fer layouts:
  - Manual: (*full custom*)
  - Automàtica (en estils semi-custom)
  - Semi-automàtica
- Editors de layout
  - Microwind
  - Virtuoso (Cadence DFII)
  - ...



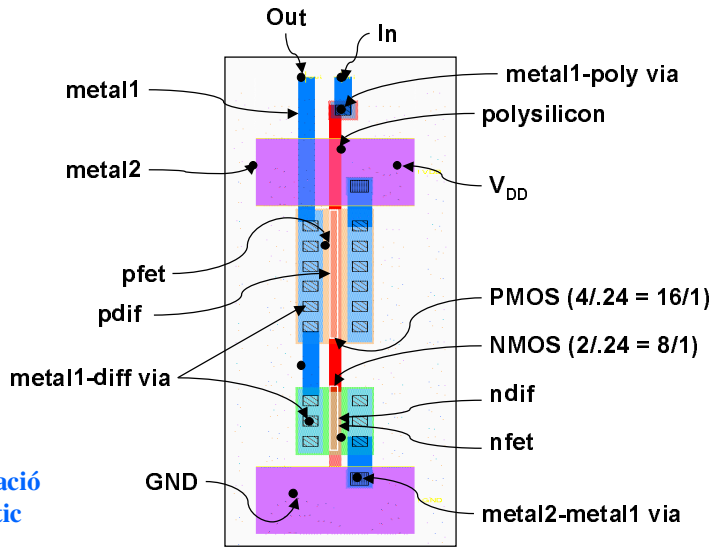
Layout

- Col·lecció de formes geomètriques dibuixades en diferents capes que representen el circuit que s'ha de construir
- La majoria són rectangles
- En un circuit de 10^9 portes: $O(10^{11})$ rectangles/capa; $O(10^{12})$ rectangles/chip

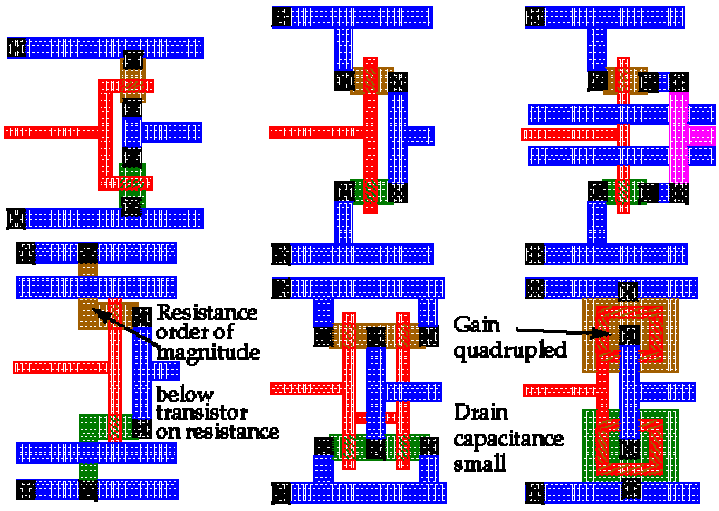




Disseny de CI: Layout

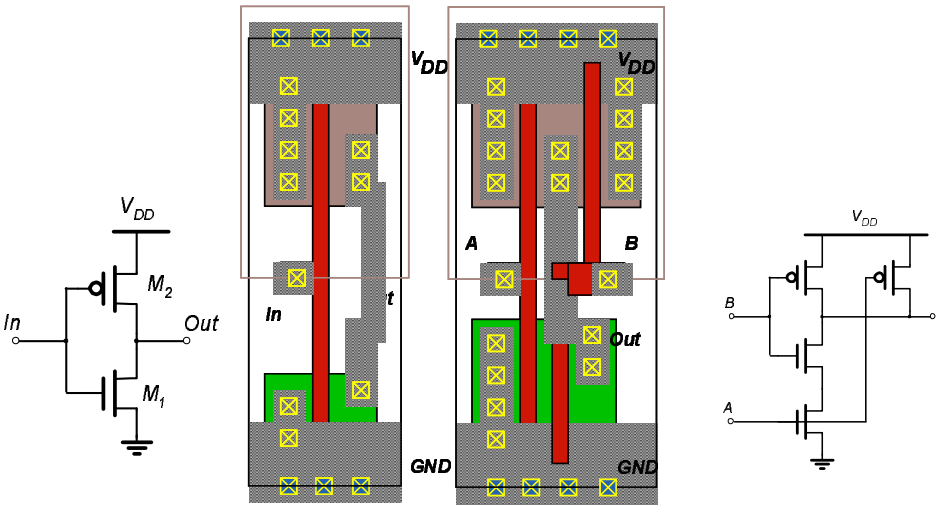


Apareix més informació
Que a un esquemàtic



Sis alternatives per un mateix circuit inversor

Layout



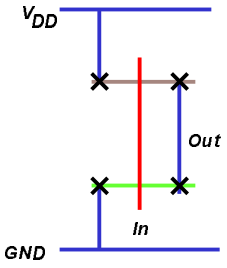
- **Warning**:

While layout is often (sometimes) fun to do, it easily can be become an infinite time sink – one can always find a way to shrink the cell a few more microns. You should really have a plan BEFORE you start layout, and have a set constraints you are trying to achieve so you know when you are done.

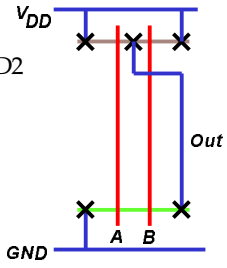
Diagrames D'sticks

No contenen mides
Representen la possició relativa dels transistors

Inverter



NAND2



Layout Issues

In CMOS there are two types of diffusion

- ndiff (green)
  - Poly crossing ndiff makes nMOS transistors
- pdiff (yellow / brown)
  - Poly crossing pdiff makes pMOS transistors

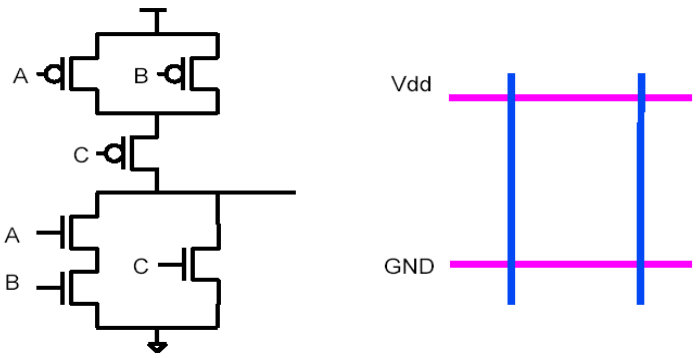
Be careful, ndiff and pdiff are different

- You can't directly connect ndiff to pdiff
  - Must connect ndiff to metal and then metal to pdiff
- Can't get ndiff too close to pdiff because of wells
  - Large spacing rule between ndiff and pdiff
  - Means you need to group nMOS devices together and pMOS devices together

Basic Layout Planning

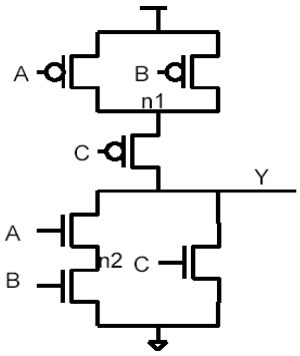
- Choose global directions for routing layers
  - Adjacent levels should route perpendicular
  - Example: m2 horizontal, m1 vertical
- Position power lines first in top layer of metal
- Cluster together NMOS with NMOS and PMOS with PMOS
- Generally keep gate orientation the same
- Arrange transistors so that common sources/drains can be shared
- Arrange transistors so that common gates line up
- Limit lengths of diffusion and poly routing – use metal
- Try to design/layout as little stuff as possible (use repetition/tools)
  - Critical issue

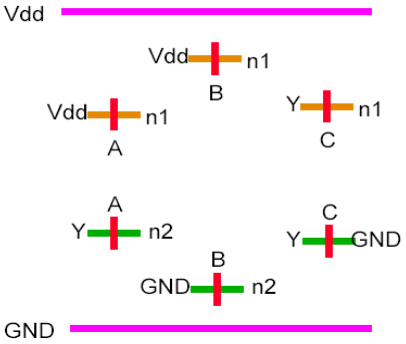
Exemple – Pas 1



- Escolliu direccions preferents pels nivells de routing

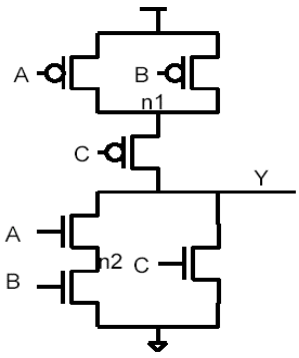
Exemple – Pas 2

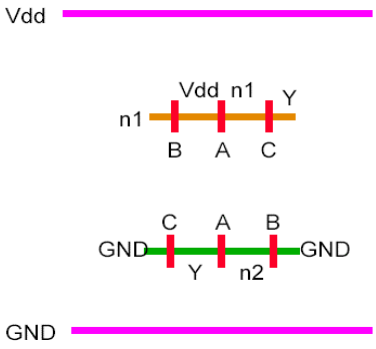




- Cluster together NMOS with NMOS and PMOS with PMOS
- Generally keep gate orientation the same

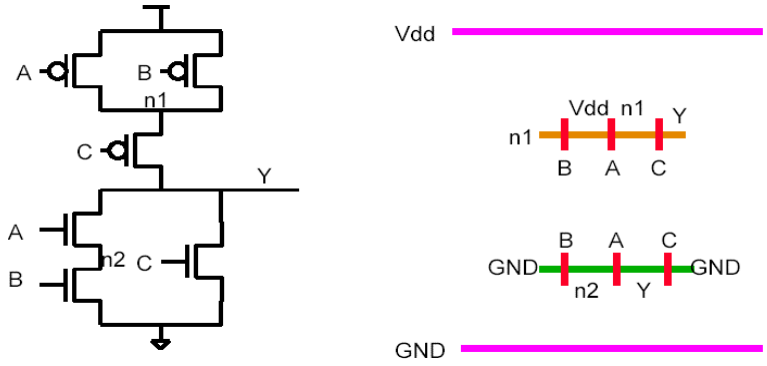
Exemple – Pas 3





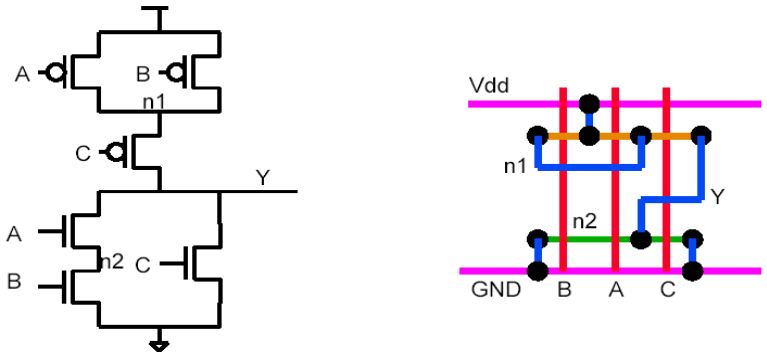
- Arrange transistors so that common sources/drains can be shared
- Give precedence to shared signals over shared vdd/ground

Exemple – Pas 4



- Arrange transistors so that common gates line up

Exemple – Pas 5



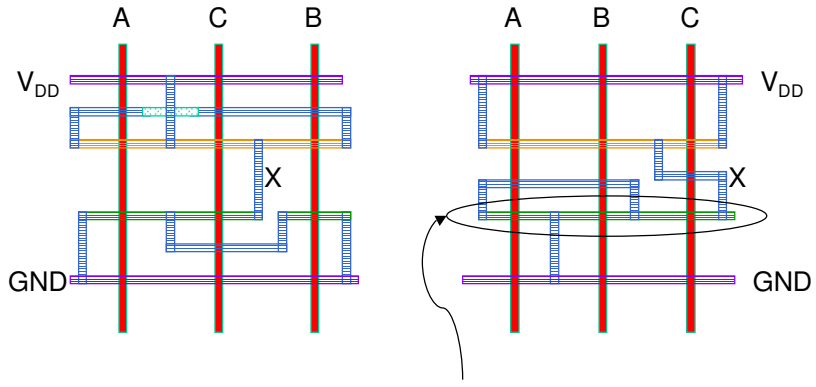
- Connect everything up

Estimating Layout Area from Sticks

- Draw your stick diagram
- Try to find the critical length path in X and in Y
- Count the number of contacted pitches
  - If transistors are not minimum width, remember to take that into account
- If you not happy with the answer, goto step 1 and try again.
  - Else you are done, and you can try to layout the cell.
- You will sometimes find out that you missed the real critical length path, but that is not unusual for people starting layout. You will get better at seeing the critical path as you do more layout.

Diagrames D'sticks

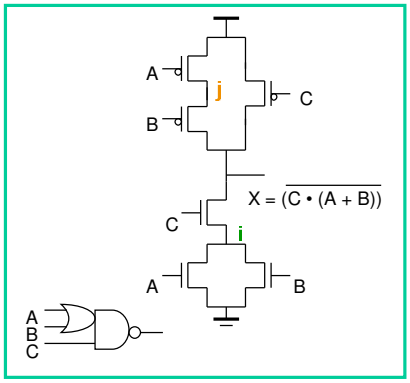
$$\overline{(C \bullet (A + B))}$$

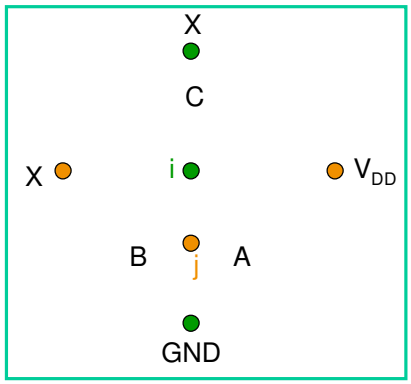


Tira de difusió sense interrupcions

Diagrames D'sticks

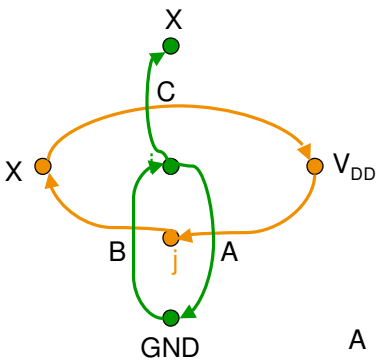
- Es possible fer el layout amb una única tira de difussió ?
  - Euler path: camí a través de tots els nusos del circuit de manera que unicament es passa una vegada per cada costat.



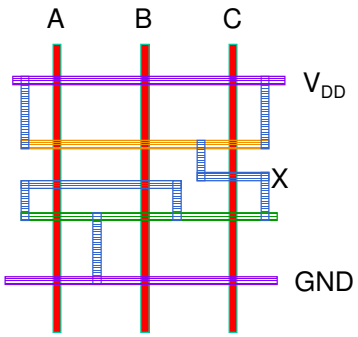


- Per a cada tira de polisilici de cada entrada, el camí d'Euler corresponents a les xarxes PUN i PDN ha de ser consistent (el mateix)

Diagrames D'sticks

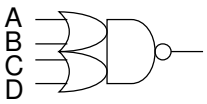


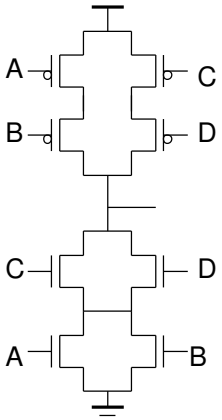
A B C



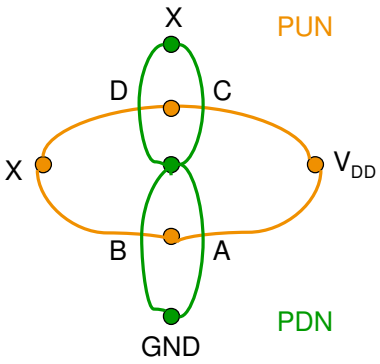
Diagrames D'sticks

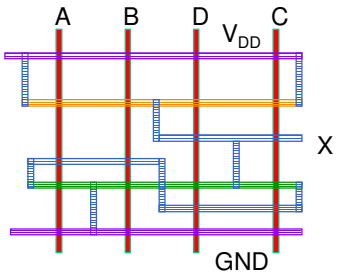
OAI22





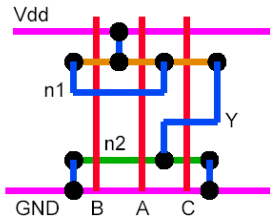
$X = \overline{((A+B)\bullet(C+D))}$

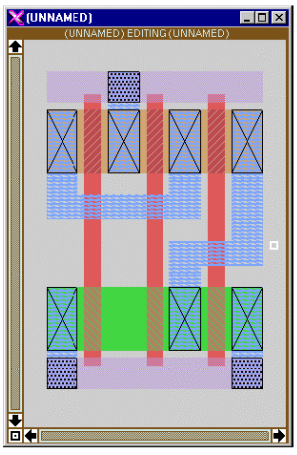




A – B – D - C

Conversió a un Layout Real



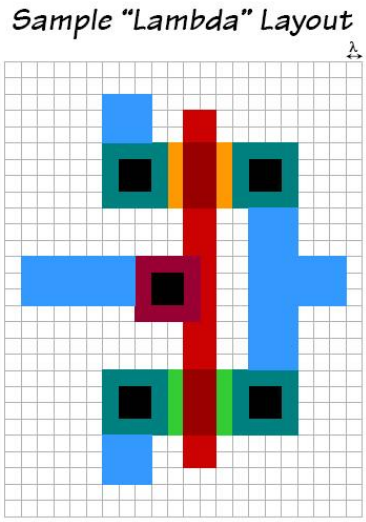


λ Lambda-based Layout

Un lambda (1λ) = La mitat de la mida mínima utilitzada per fer les màscares, típicament la longitud de canal del transistor

Generalment, tots els polígons han de trobar-se “on grid”,

e.g., Al Microwind el pas de la retícula és de 1λ.



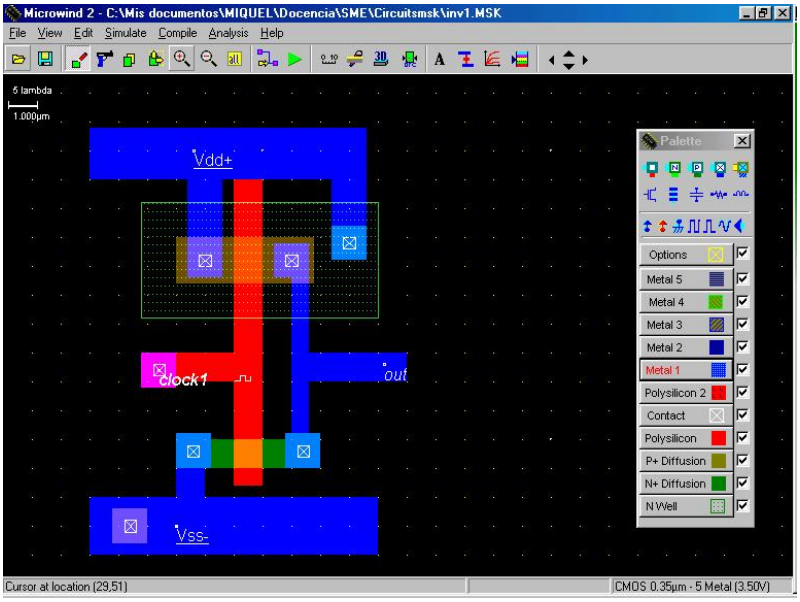
- 2.1. Eina Microwind

Disseny full custom

- Eina : Microwind (v3)
- Inclou un Editor de Layout
- Tecnologia :
  - CMOS 1.2um
  - CMOS 0.8um
  - CMOS 0.6um
  - CMOS 0.35um
  - CMOS 0.25um
  - CMOS 0.18um
  - CMOS 0.12um
  - CMOS 90n
  - CMOS 70n
  - CMOS 50n

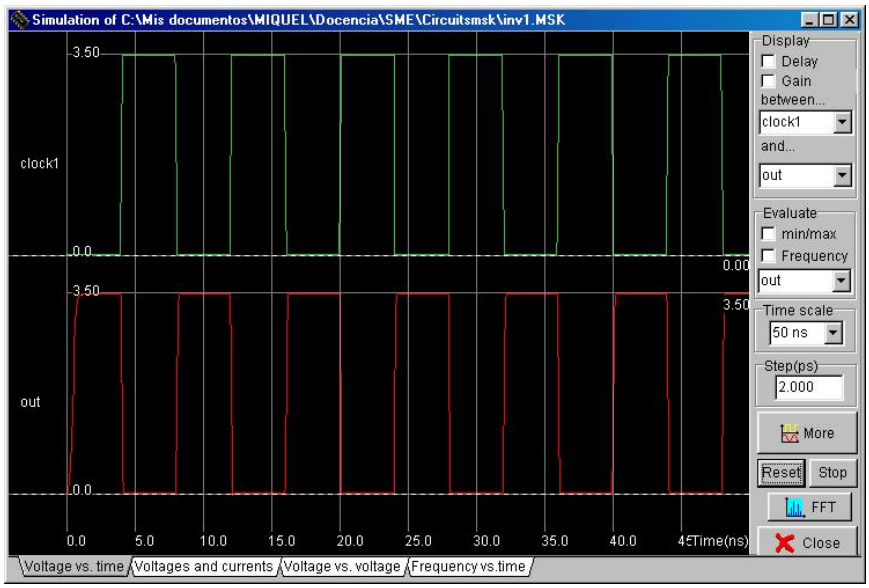
Conjunt de màscares de microwind

Editor de layout

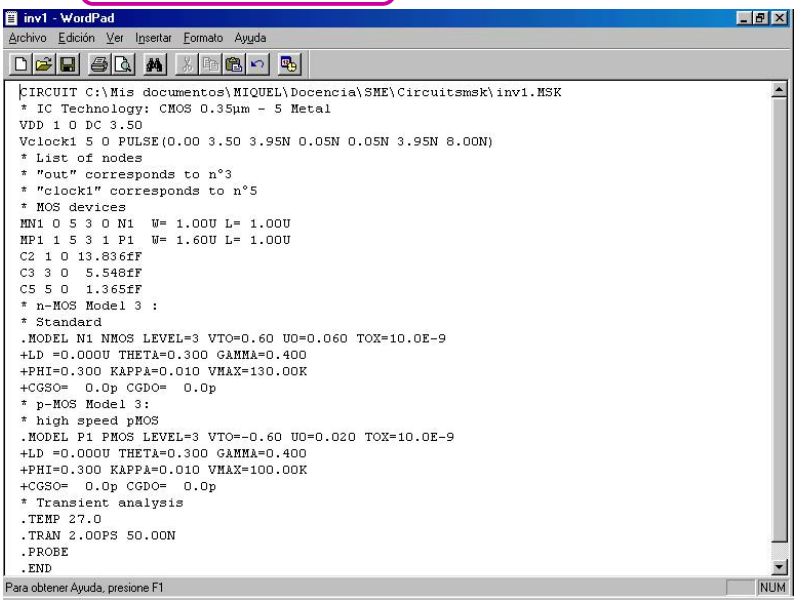


Inversor CMOS

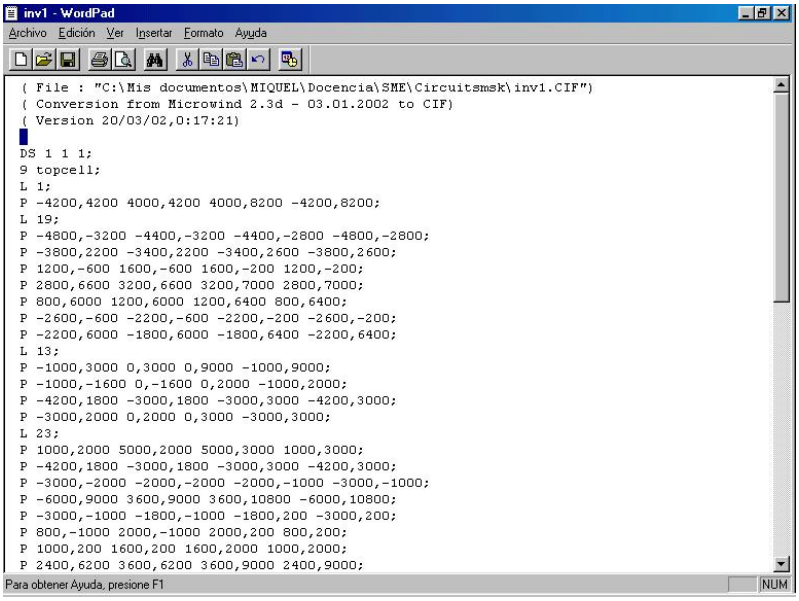
Simulació Elèctrica



Extracció Spice



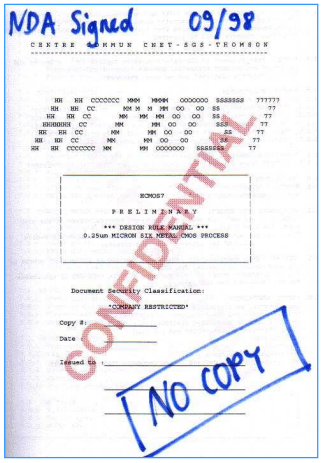
Extracció CIF



- 2.2. Regles de Disseny

Regles de disseny

- Relació enginyer proces i enginyer disseny
- Normes per construir les màscares (limitacions)
- Dimensió : Mínima amplada de línea
  - regles de disseny escalables :
    - Parametritzades - Unitats de lambda (λ) :
    - Longitud mínima canal = 2 (λ)
  - dimensions absolutes (no escalable)
    - Unitats de micres

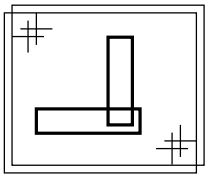


Confidencial-Acord-No copiable

Per què es necessiten Regles de Disseny?

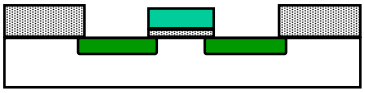
- Per poder tolerar alguns petits errors del procés de fabricació:

1. Desalineament de màscares



2. Pols

3. Paràmetres del process (e.g., lateral diffusion)



4. Superficies rugoses

CMOS 0.35µm - 5 Metal

*

lambda = 0.2

(Lambda is set to half the gate size)

metalLayers = 5 (Number of metal layers : 5)

*

* Design rules associated to each layer

*

* Well (Gds2 level 1)

r101 = 10 (well width)

r102 = 11 (well spacing)

*

* Diffusion (N+ 16, P+ 17, active 2)

r201 = 4 (diffusion width)

r202 = 4 (diffusion spacing)

r203 = 6 (border of nwell on diffp)

r204 = 6 (nwell to next diffn)

r205 = 3 (distance diffn/diffp)

*

* Poly (13)

r301 = 2 (poly width)

r302 = 2 (gate length)

r304 = 3 (poly spacing)

r305 = 1 (spacing poly and unrelated diff)

r306 = 4 (width of drain and source diff)

r307 = 2 (extra gate poly)

* Contact (19)

r401 = 2 (contact width)

r402 = 3 (contact spacing)

r403 = 2 (metal border for contact)

r404 = 2 (poly border for contact)

r405 = 2 (diff border for contact)

*

* Metal 1 (23)

r501 = 3 (metal width)

r502 = 3 (metal spacing)

*

* via (25)

r601 = 2 (Via width)

r602 = 3 (Spacing)

r603 = 0 (via/contact)

r604 = 2 (border of metal&metal2)

*

*metal 2 (27)

r701 = 4 (Metal 2 width)

r702 = 4 (spacing)

*

* via 2 (32)

r801 = 2 (Via width)

r802 = 3 (Spacing)

r804 = 2 (border of metal2&metal3)

*

· metal 3 (34)

r901 = 4 (width)

r902 = 4 (spacing)

* via 3 (35)

ra01 = 2 (Via width)

ra02 = 3 (Spacing)

ra04 = 2 (border of metal3&metal4)

*

* metal 4 (36)

rb01 = 4 (width)

rb02 = 4 (spacing)

*

* via 4 (52)

rc01 = 2 (Via width)

rc02 = 3 (Spacing)

rc04 = 2 (border of metal4&metal5)

* metal 5 (53)

rd01 = 4 (width)

rd02 = 10 (spacing)

*

* Passivation nitride (31) and pad rules

rp01 = 550 (Pad width)

rp02 = 550 (Pad spacing)

rp03 = 25 (Border of Vias)

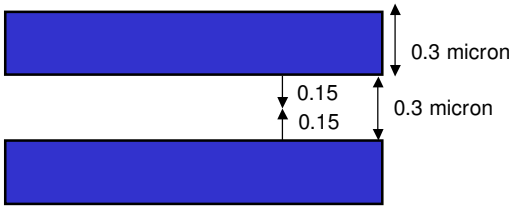
rp04 = 25 (Border of metals)

rp05 = 150 (to unrelated active areas)

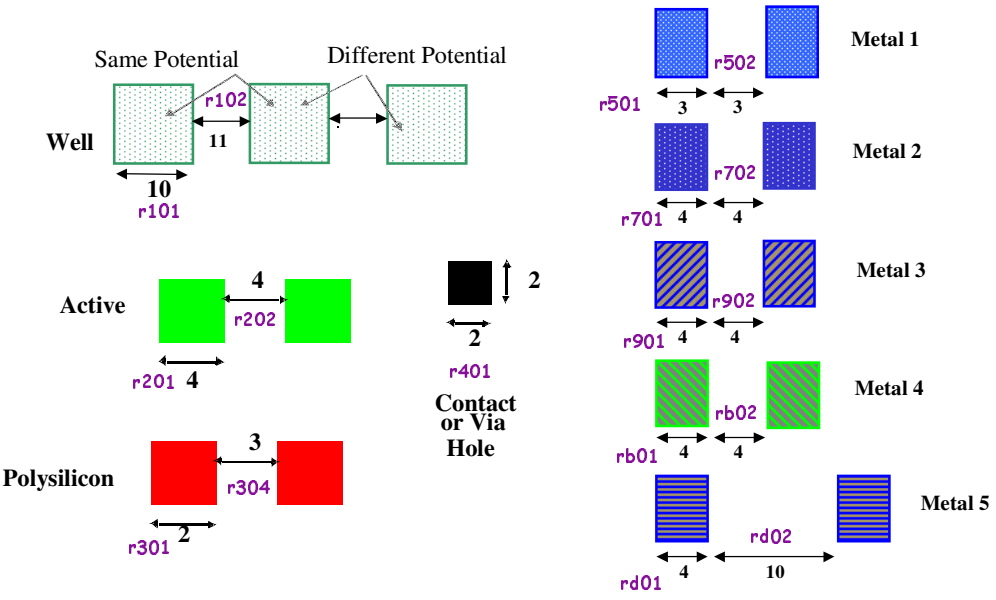
*

Intra-Layer Design Rule Origins

- Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
  - minimum line width is set by the resolution of the patterning process (photolithography)
- Minimum spaces between objects (that are *not* related) on the same layer to ensure they will not short after fab



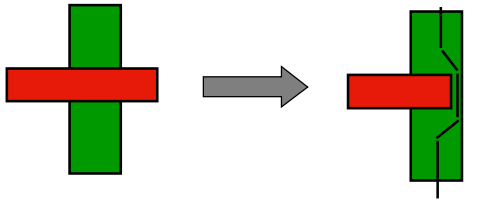
Intra-Layer Design Rules



Inter-Layer Design Rule Origins

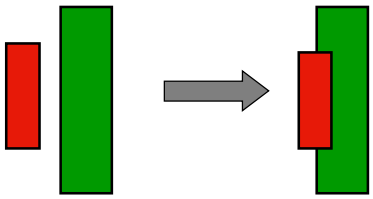
1. Transistor rules – transistor formed by overlap of active and poly layers

Transistors

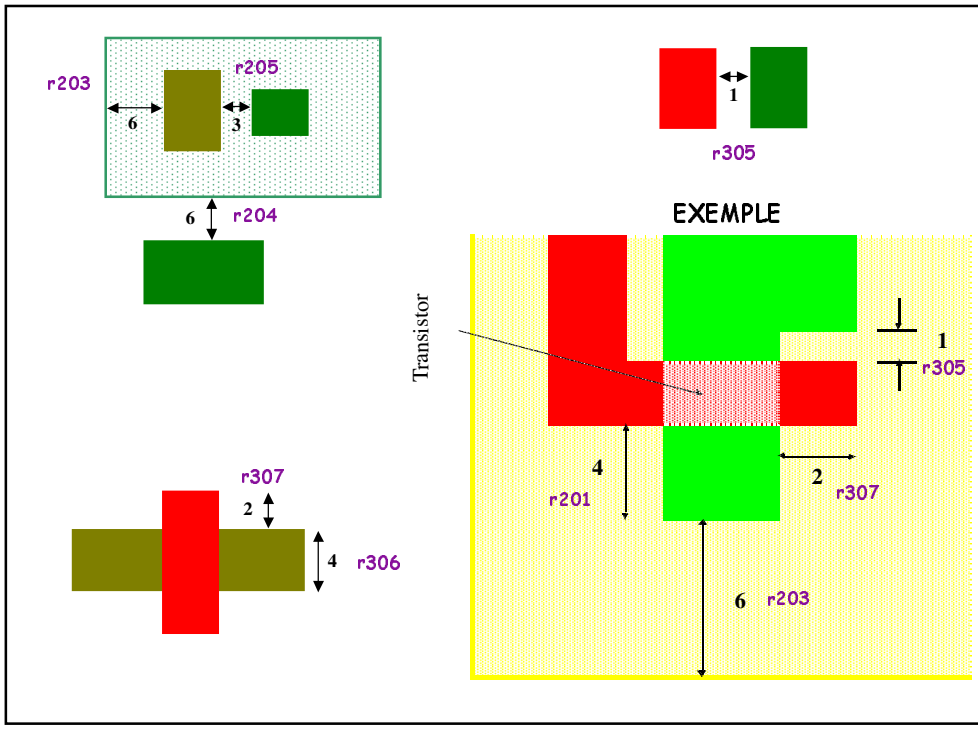


Catastrophic error

Unrelated Poly & Diffusion



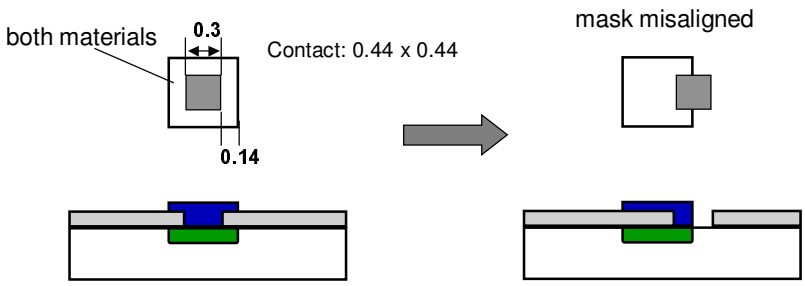
Thinner diffusion, but still working



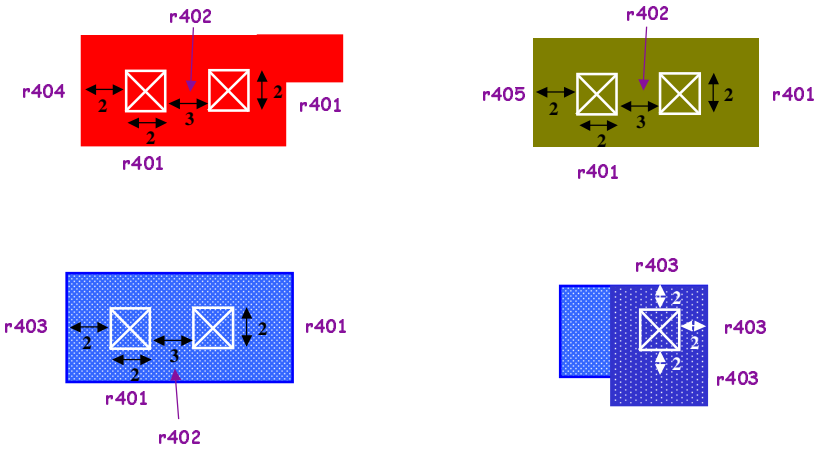
Inter-Layer Design Rule Origins, Con't

2. Contact and via rules

M1 contact to p-diffusion M1 contact to n-diffusion M1 contact to poly	Contact Mask
Mx contact to My	Via Masks

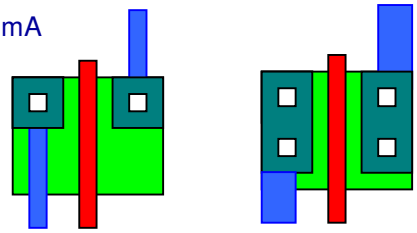


Regles de disseny: CMOS 0.35um



Regles de disseny: CMOS 0.35um

- Altres consideracions (de tipus més elèctric)
  - Contactes als drenadors i sortidors de transistors grans
    - vies normalment 1mA

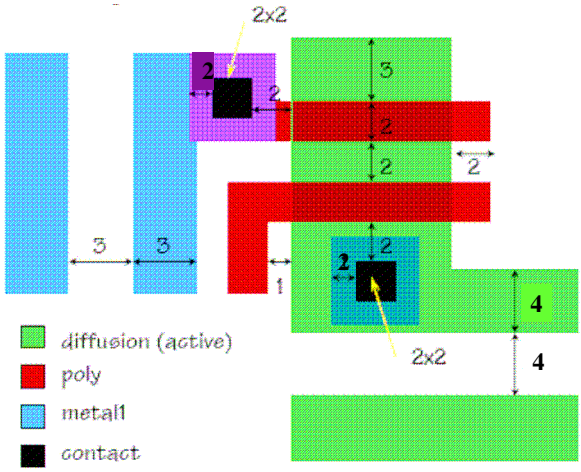


  - Dimensionat de les pistes de VDD-GND
    - electromigració
    - metals entre 1.5mA/um i 3 ma/um depenent del nivell
  - Polaritzacions de POU i Substrate
    - evitar efecte resistiu de les pistes (possible renou i degradació)

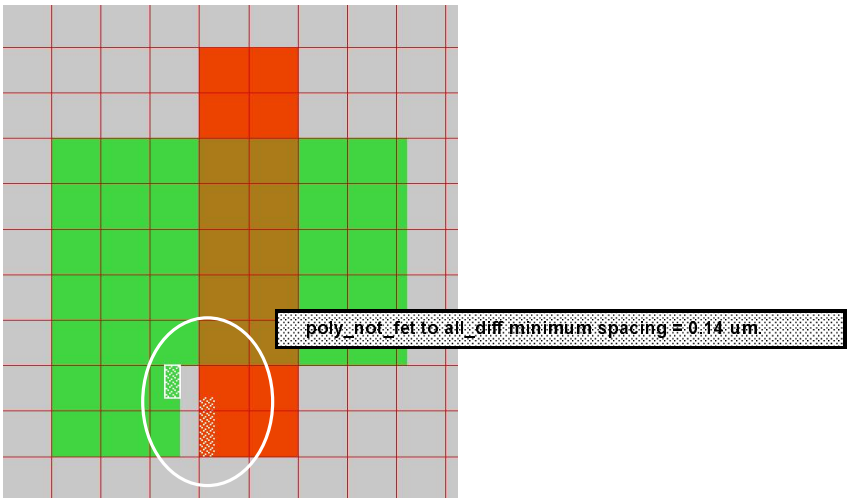
Exercici

Identifiqueu les regles de disseny
Que apareixen en aquest layout

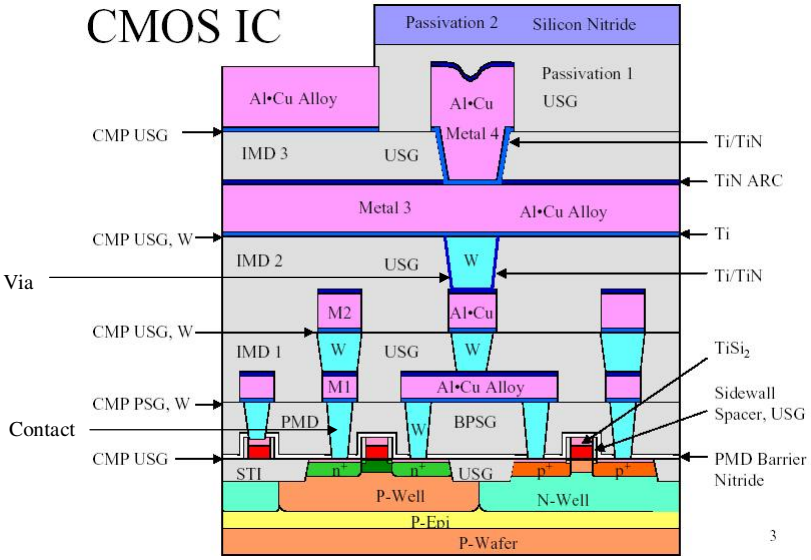
Hi ha alguna regla que No aparegui a la llista?



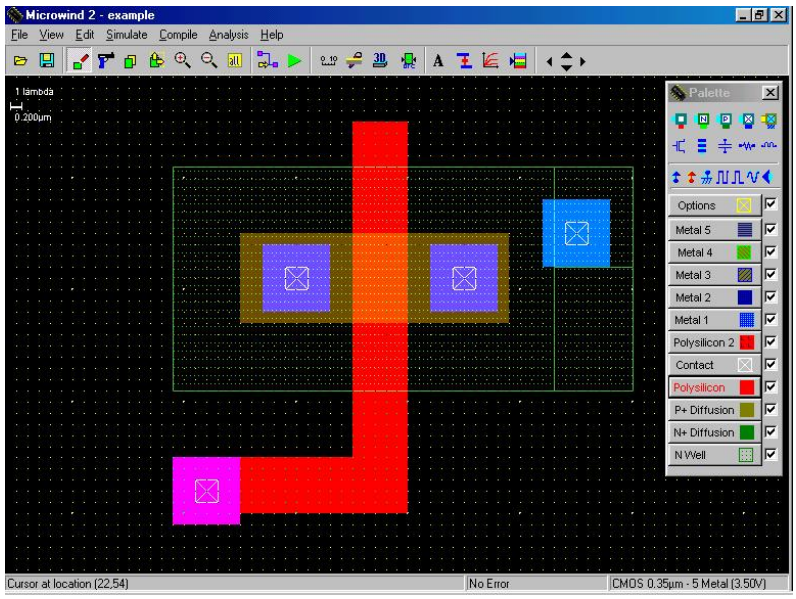
Design Rule Checker



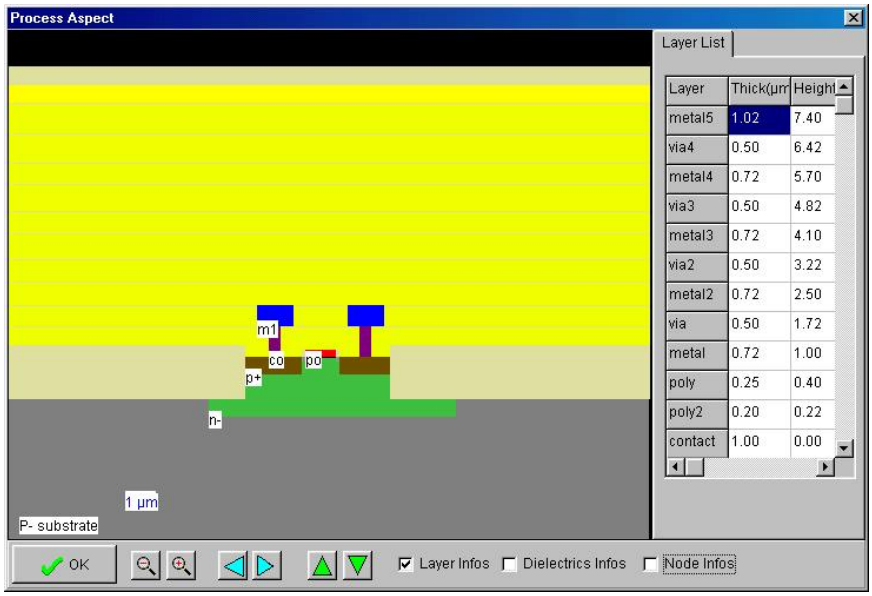
Seccions transversals



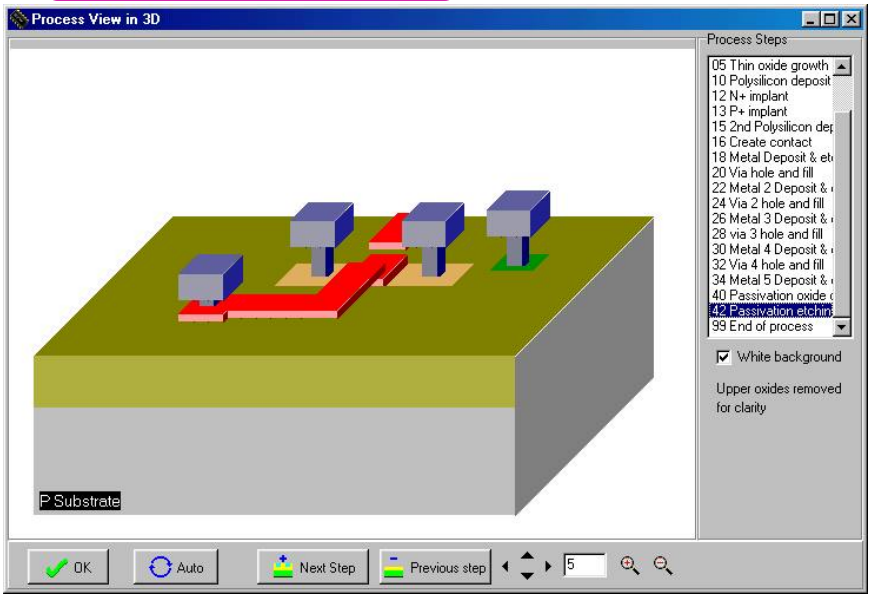
FC. Transistor PMOS



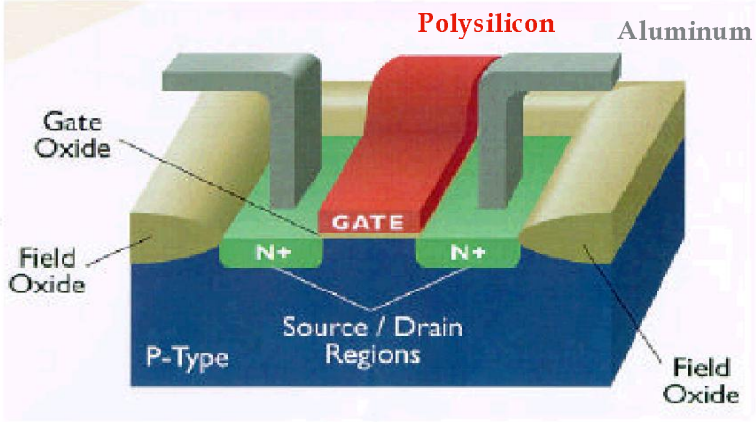
FC. PMOS Tall transversal



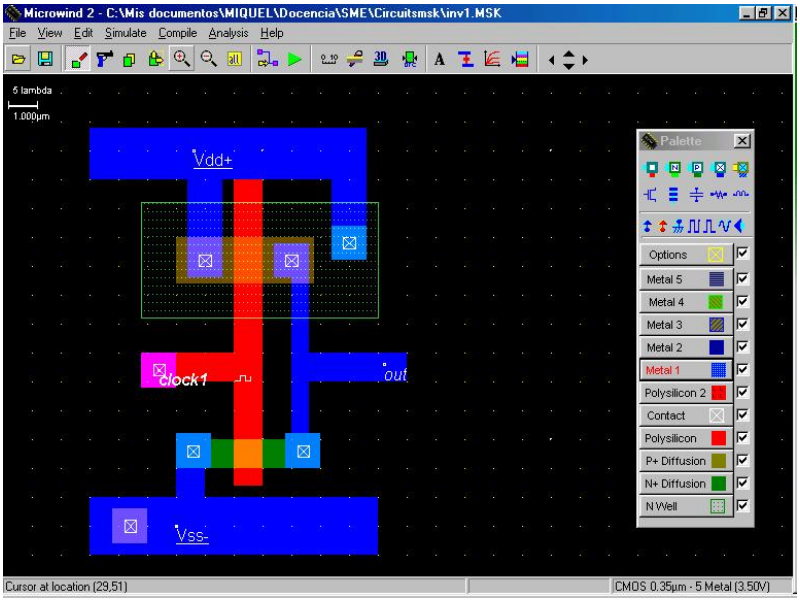
FC. PMOS. Vista 3D



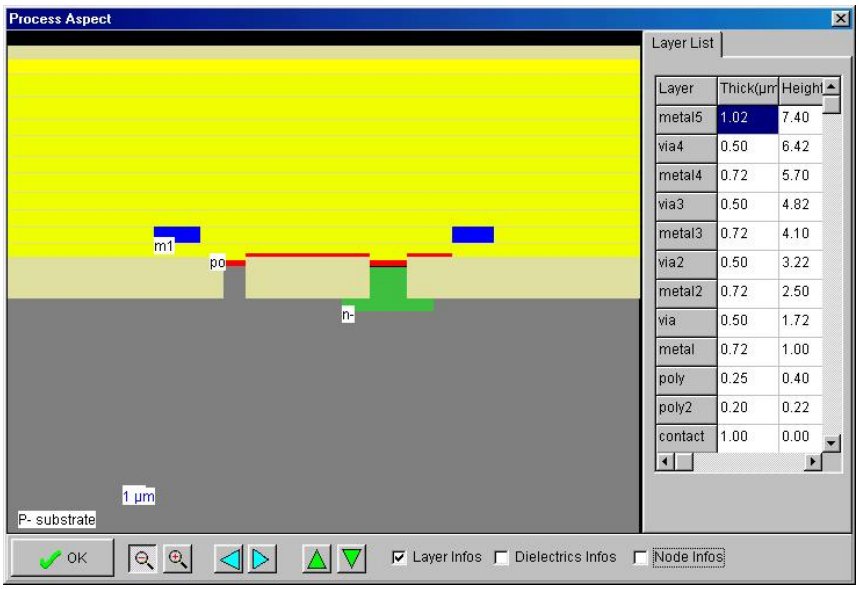
3D Perspective



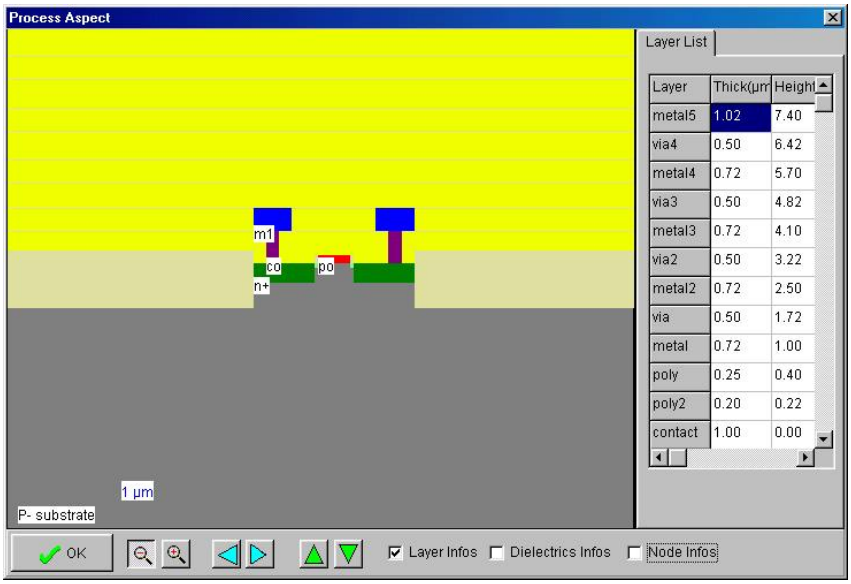
Inversor CMOS



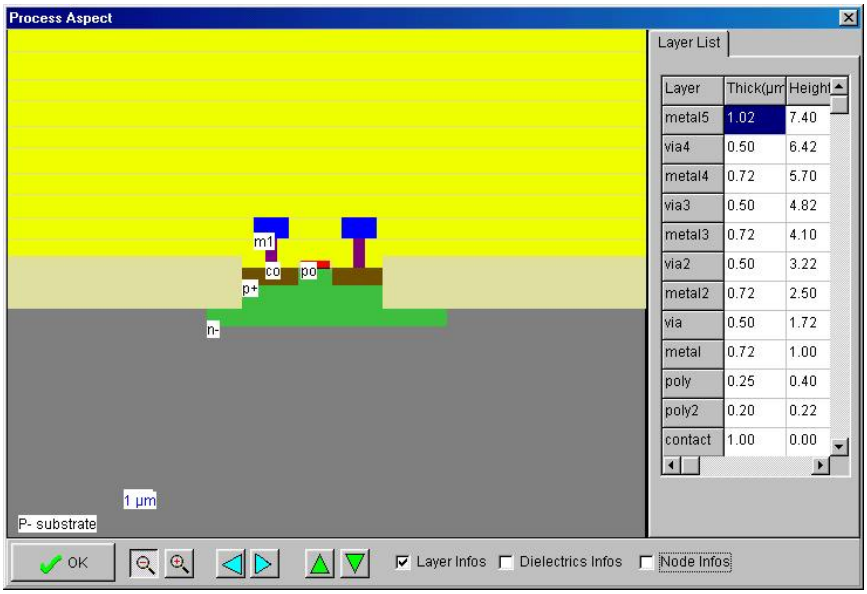
Tall vertical



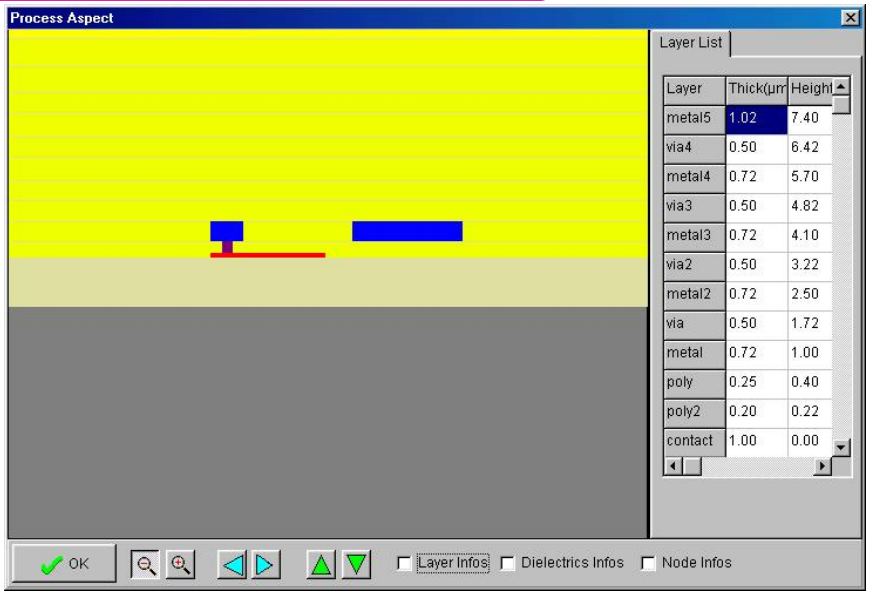
Tall horitzontal NMOS



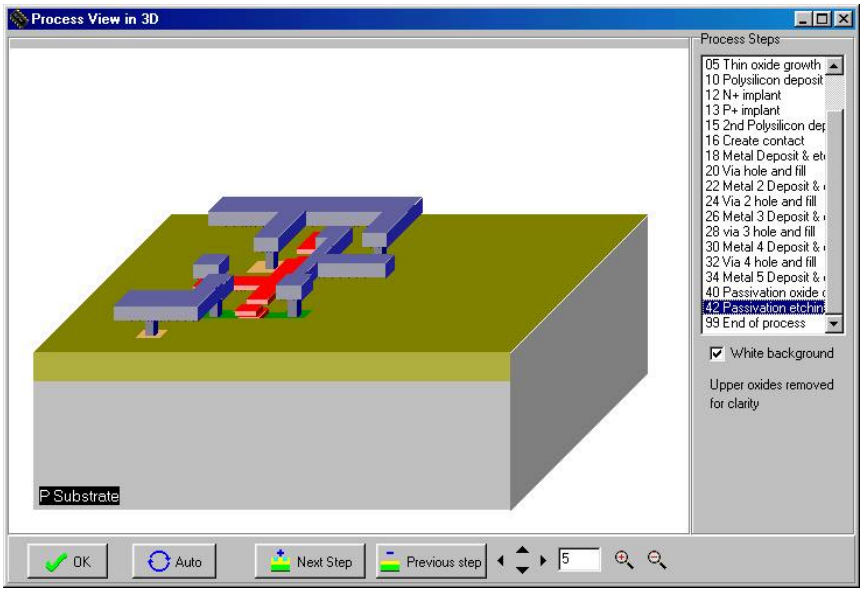
Tall horitzontal PMOS



Tall horitzontal metal-polisilici



Inversor 3D


Process View in 3D
Process Steps
05 Thin oxide growth
10 Polysilicon deposit
12 N+ implant
13 P+ implant
15 2nd Polysilicon dep
16 Create contact
18 Metal Deposit & et
20 Via hole and fill
22 Metal 2 Deposit &
24 Via 2 hole and fill
26 Metal 3 Deposit &
28 via 3 hole and fill
30 Metal 4 Deposit &
32 Via 4 hole and fill
34 Metal 5 Deposit &
40 Passivation oxide
42 Passivation etchin
99 End of process
White background
Upper oxides removed for clarity
P Substrate
OK
Auto
Next Step
Previous step
5