

Electrónica Digital
1^{er} Curso Ingeniería Técnica Industrial
(Electrónica Industrial)

Memorias de Semiconductor

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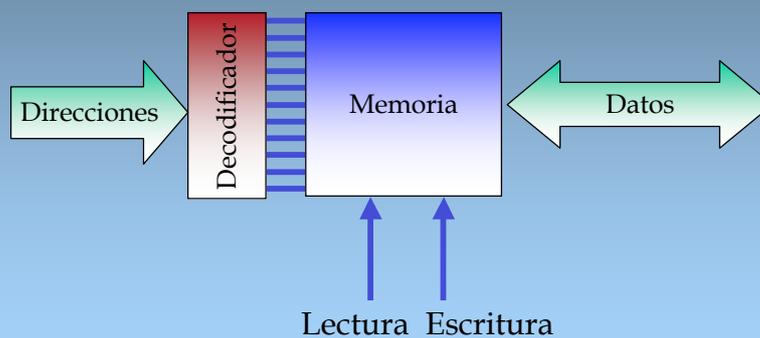
Índice

- Conceptos básicos
- Memorias de acceso aleatorio (RAM)
- Memorias de sólo lectura (ROM)
- Memorias EPROM y EEPROM

Introducción

- Memorias: Matrices de elementos que almacenan datos binarios
- Organizadas en bytes (grupos de 8 bits)
- Elemento básico que almacena un bit se le llama celda
- Unidades de almacenamiento:
 - Kbits 2^{10} bits = 1024 bits
 - Kbytes 2^{10} bytes = 1024 bytes = 8192 bits
 - Mbytes 2^{20} bytes = 1048576 bytes

Diagrama de bloques



Memorias Semiconductoras

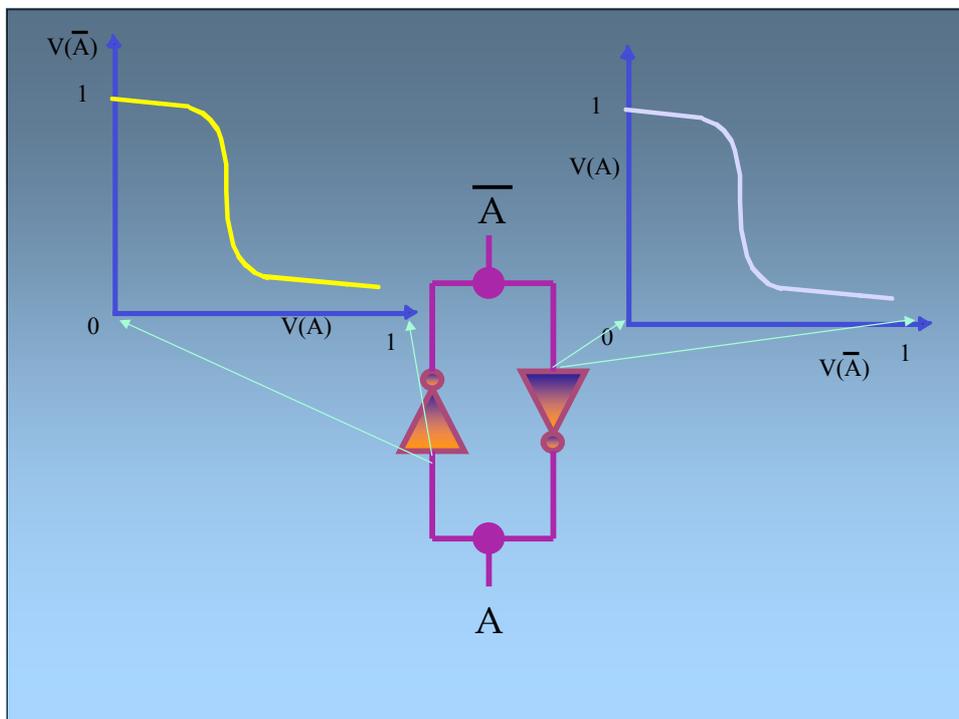
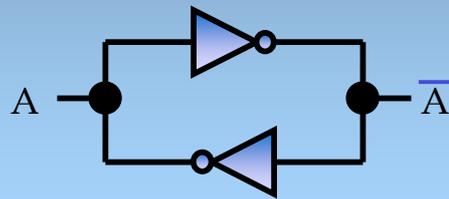
- Memorias RAM
 - Random-Access Memory
 - Con capacidad de lectura y escritura
 - Volátiles (pierden la memoria al desconectarse)
 - Se tarda lo mismo en acceder cualquier posición
- ROM
 - Read-Only Memory
 - Sólo con capacidad de lectura
 - No volátiles (mantienen la memoria al desconectarse)

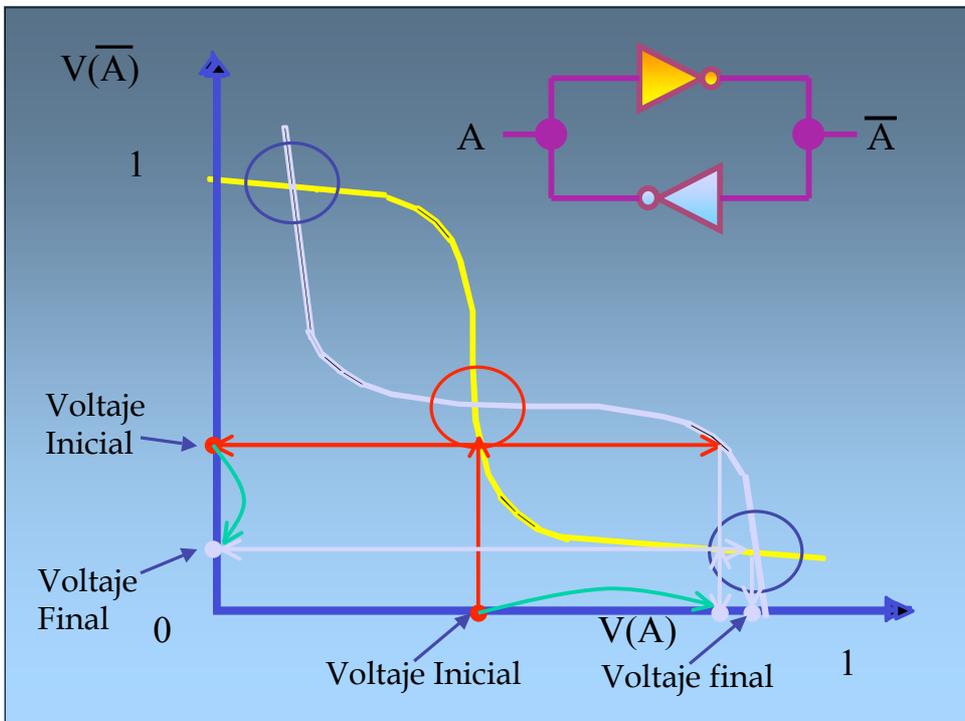
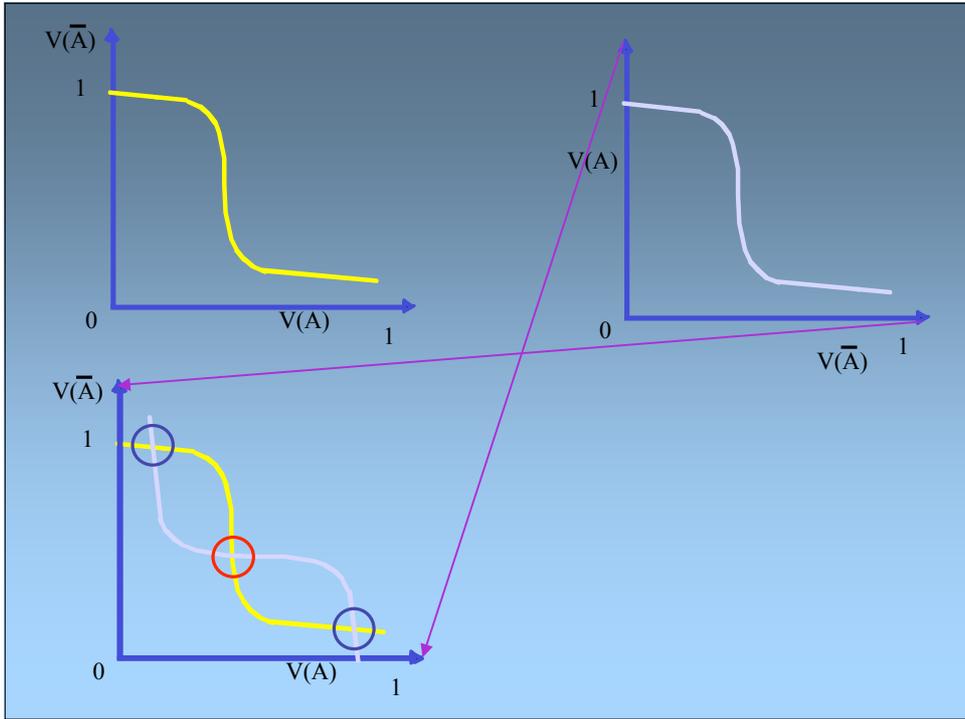
Familia de memorias RAM

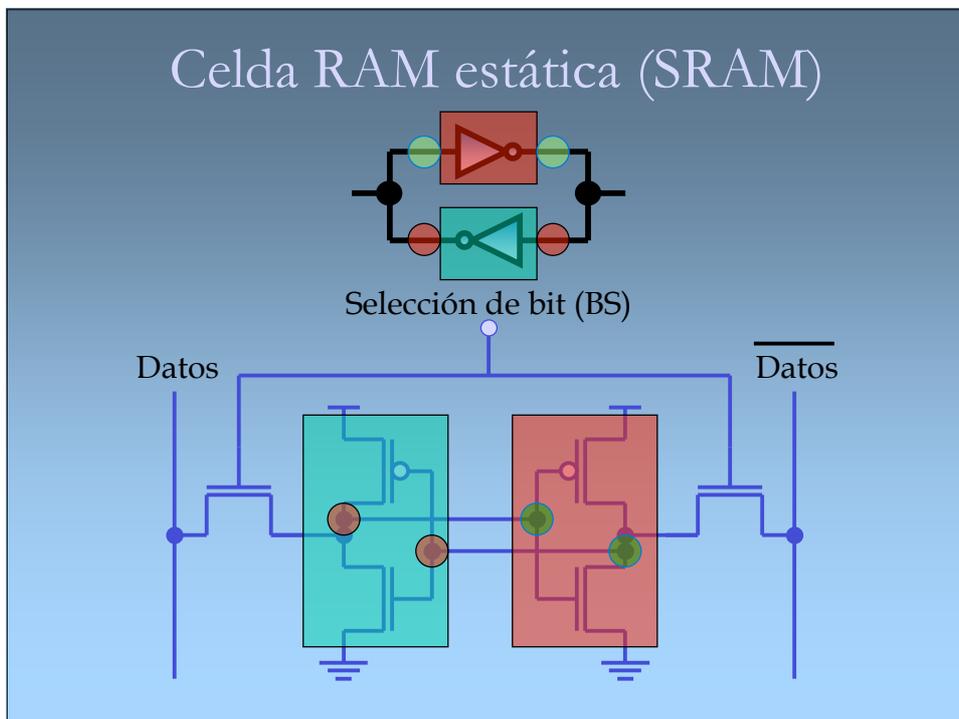
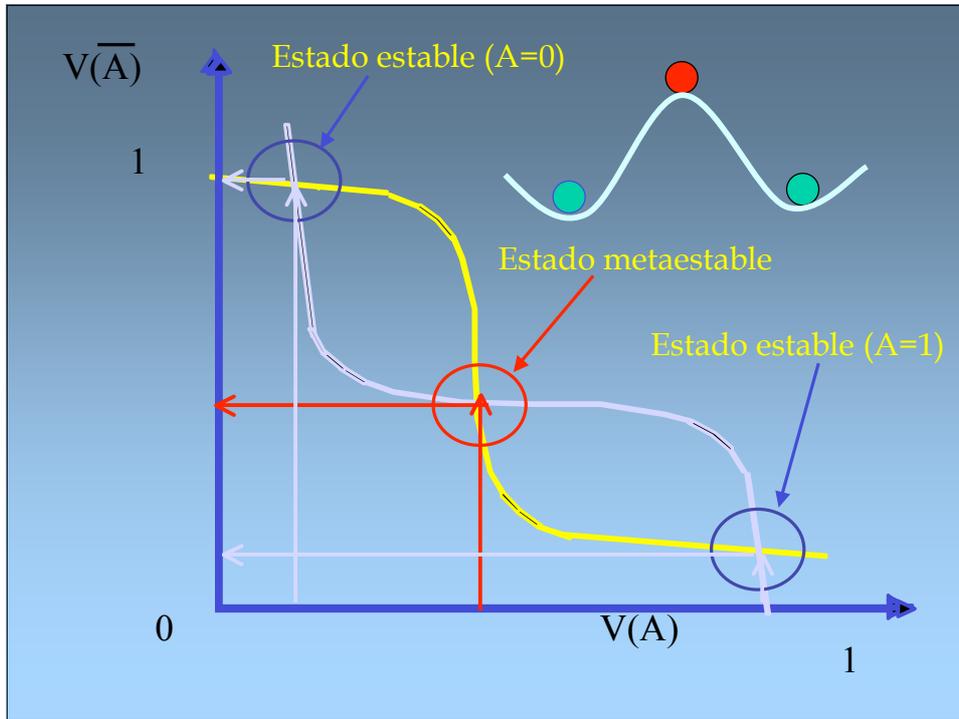
- RAM estática (SRAM)
 - Asíncrona
 - De ráfaga síncrona
- RAM dinámica (DRAM)
 - Fast-Page Mode
 - EDO DRAM
 - BEDO DRAM
 - Síncrona (SDRAM)

Celda SRAM

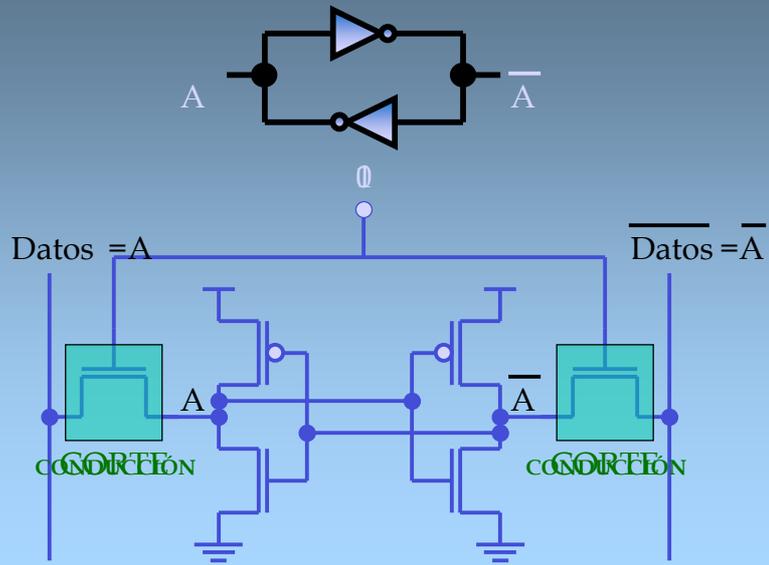
- Esquema de realimentación básico
 - No tiene ninguna entrada
 - Mantiene el estado ($A=0$ ó $A=1$) indefinidamente





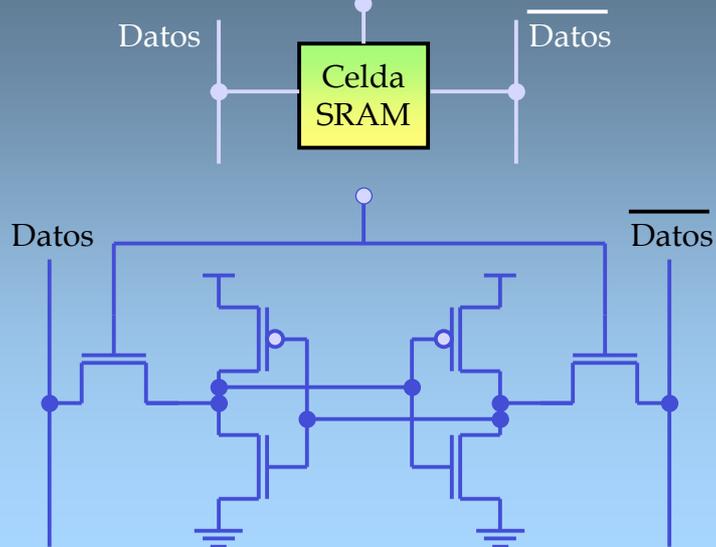


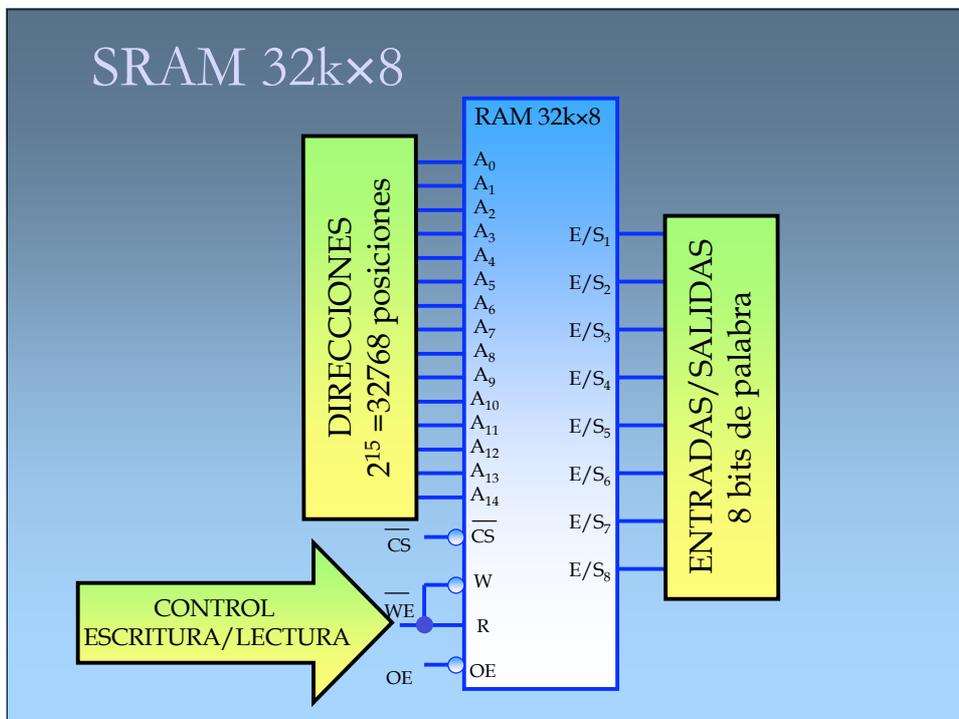
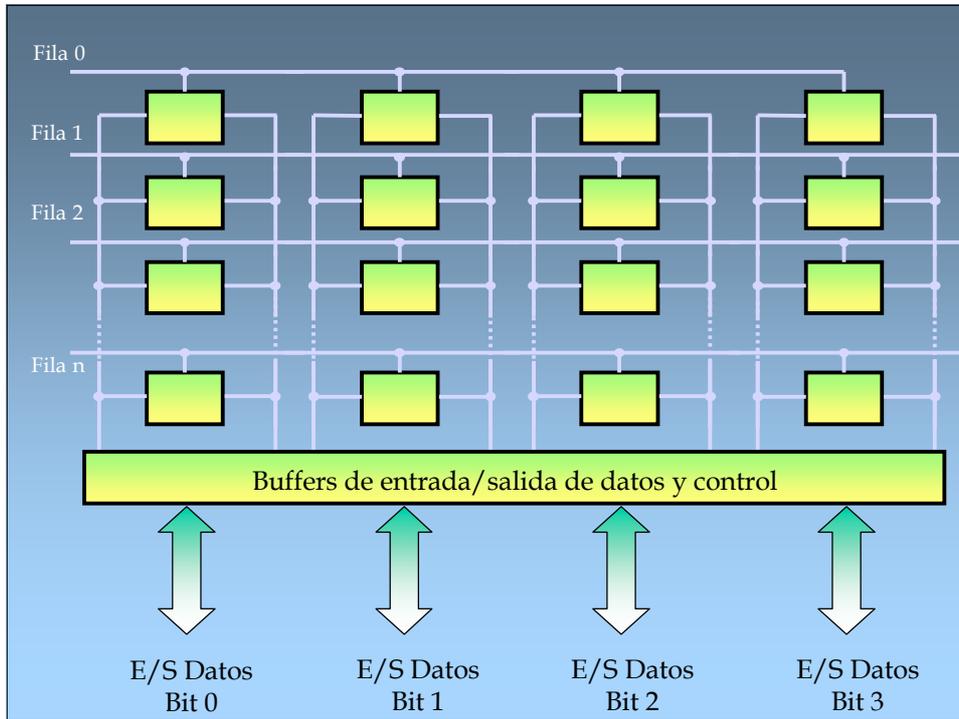
Celda RAM estática (SRAM)



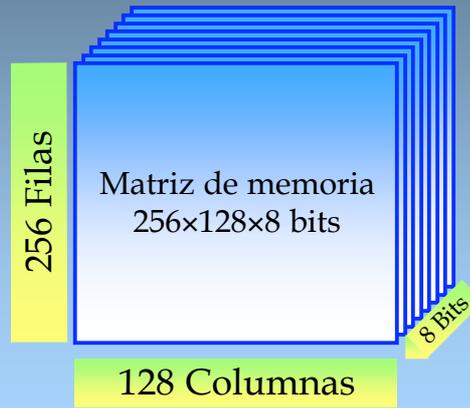
Celda RAM estática (SRAM)

Selección de datos

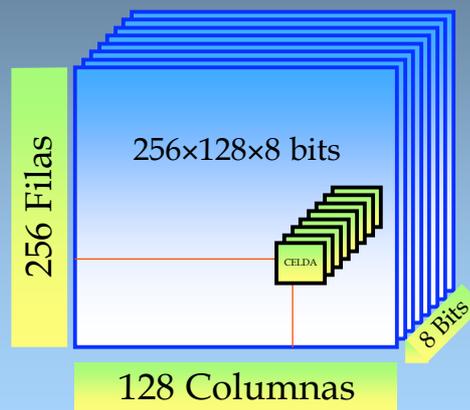




SRAM 32k×8



SRAM 32k×8



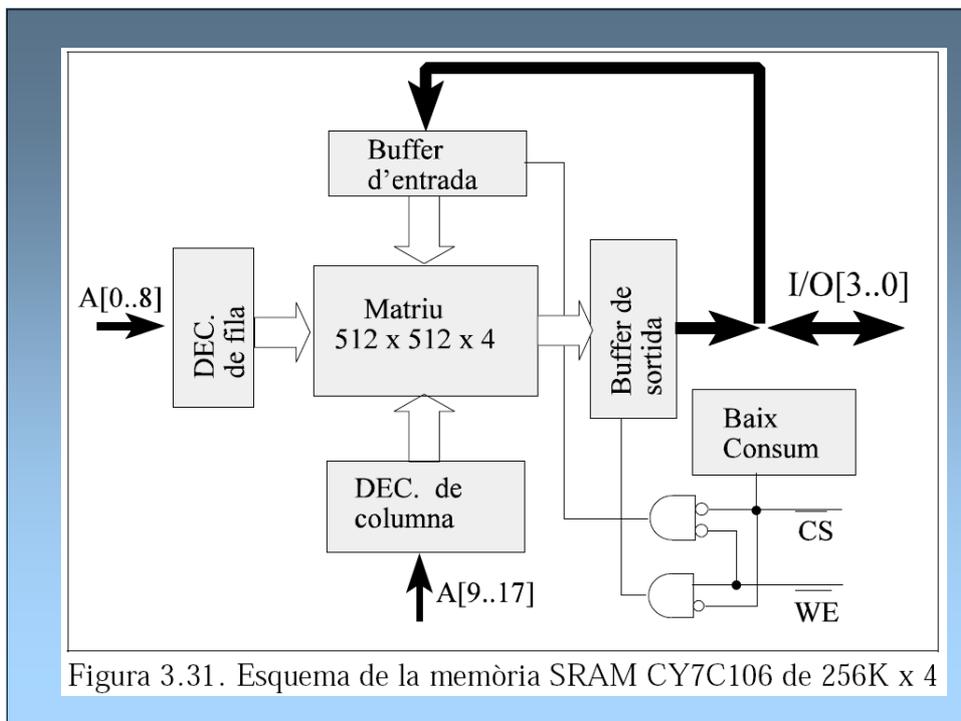
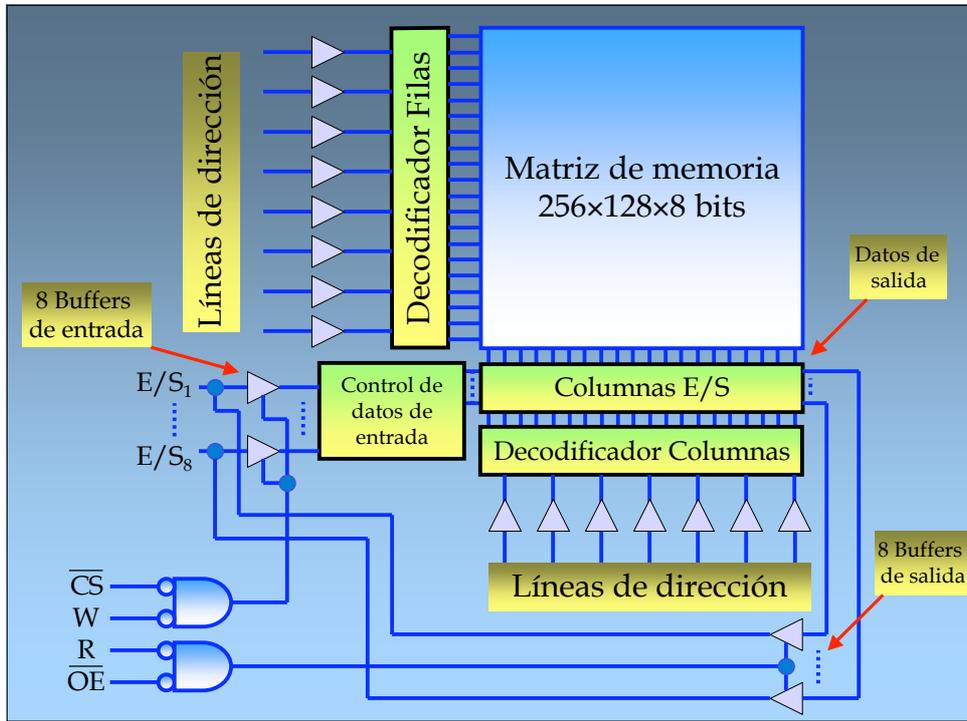
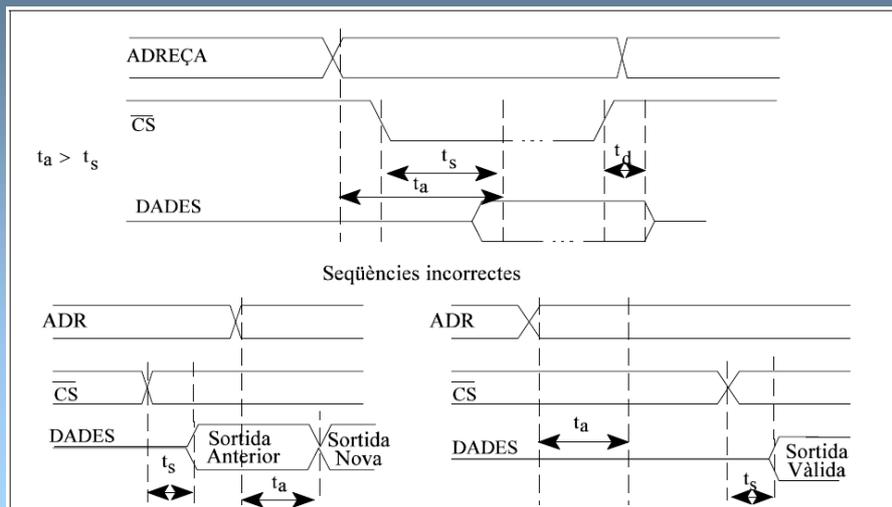
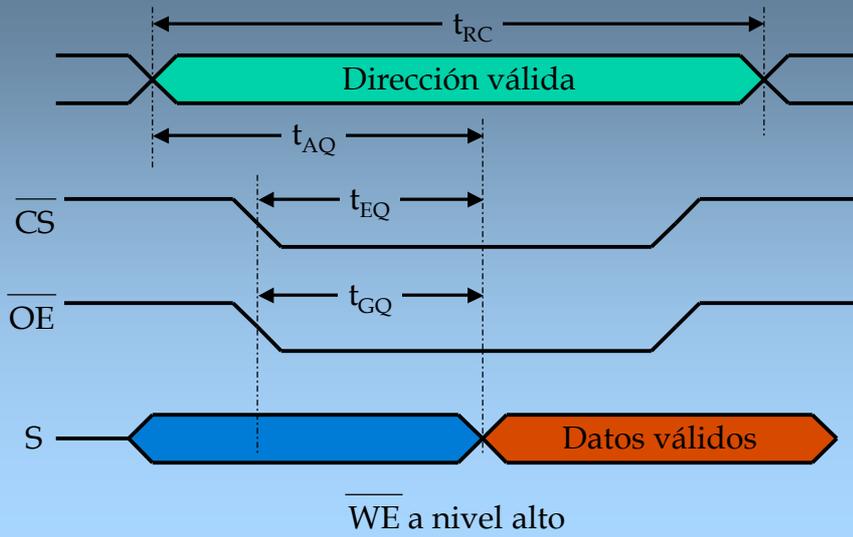
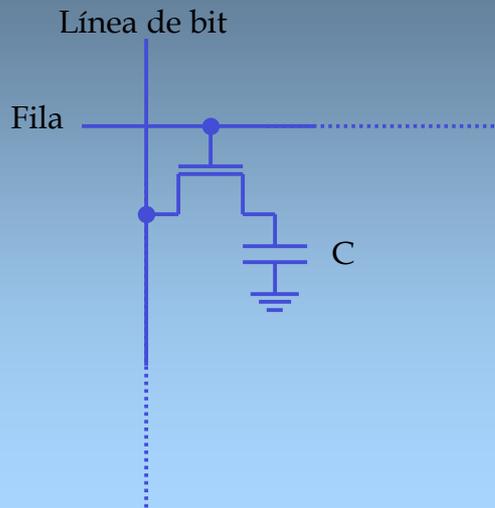


Figura 3.31. Esquema de la memòria SRAM CY7C106 de 256K x 4

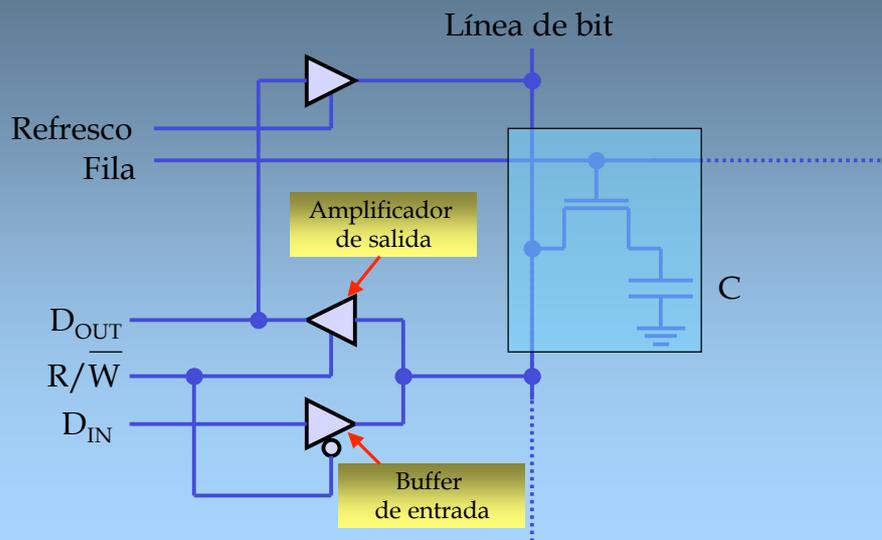
Proceso de lectura



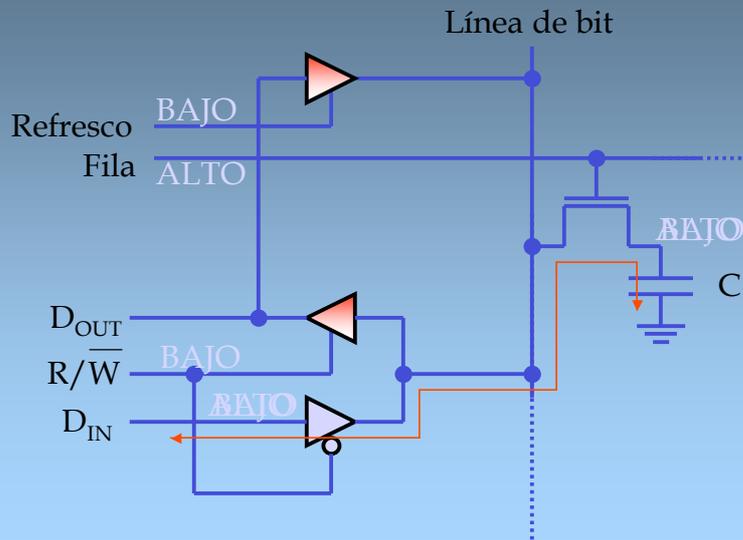
Celda DRAM



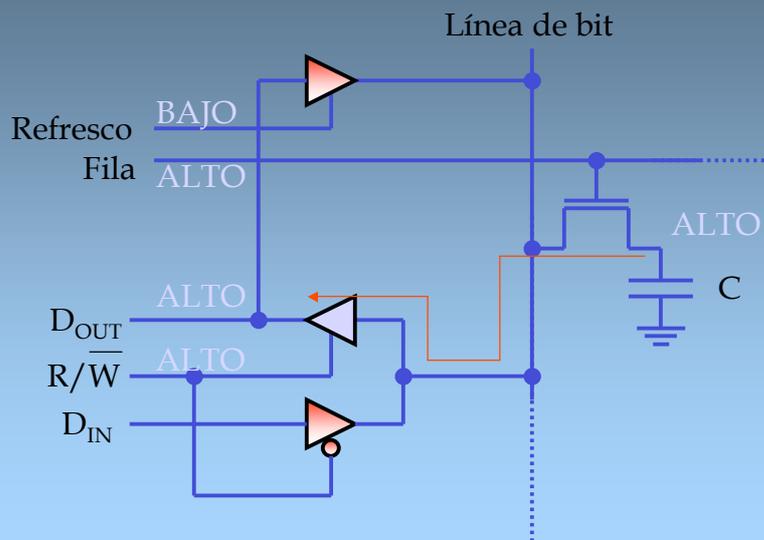
Celda DRAM



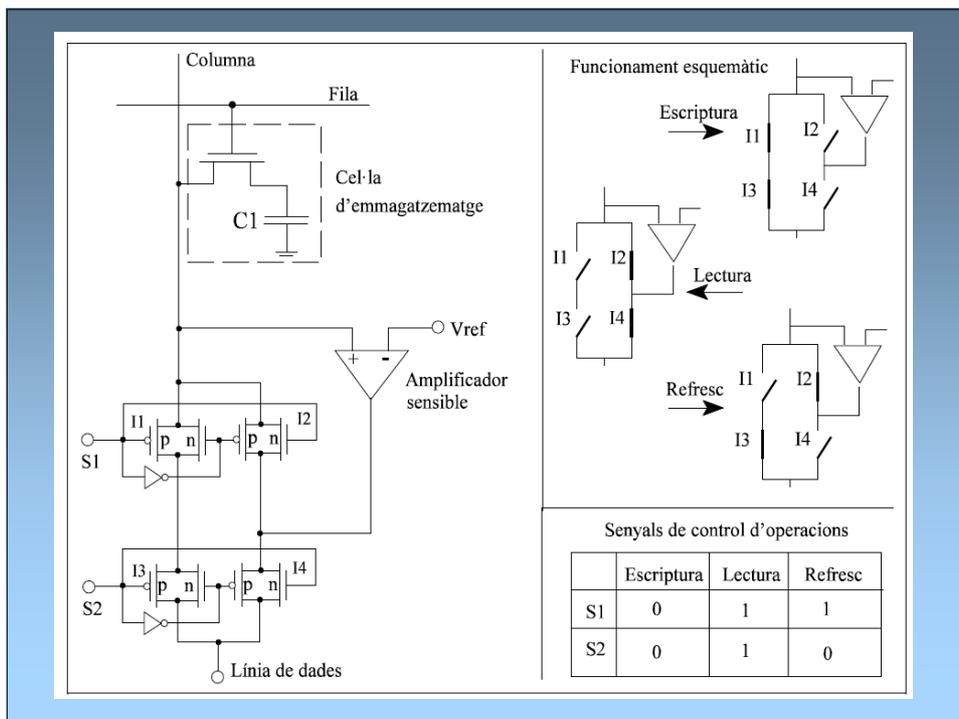
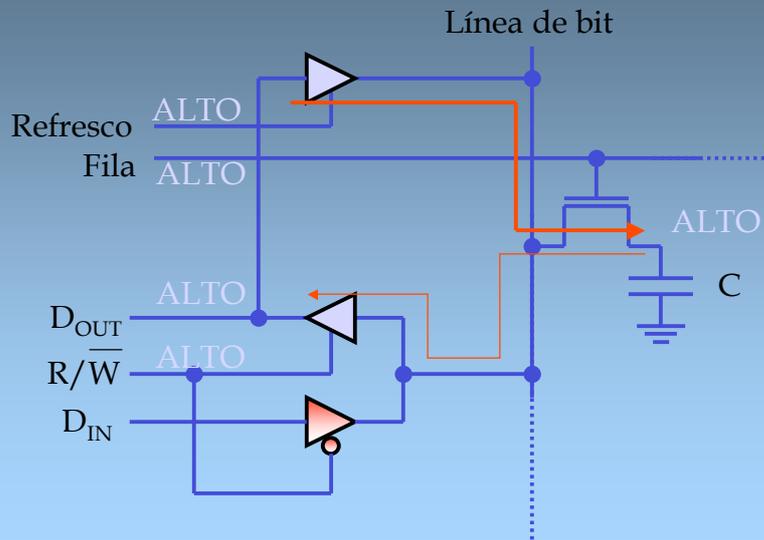
Proceso de escritura

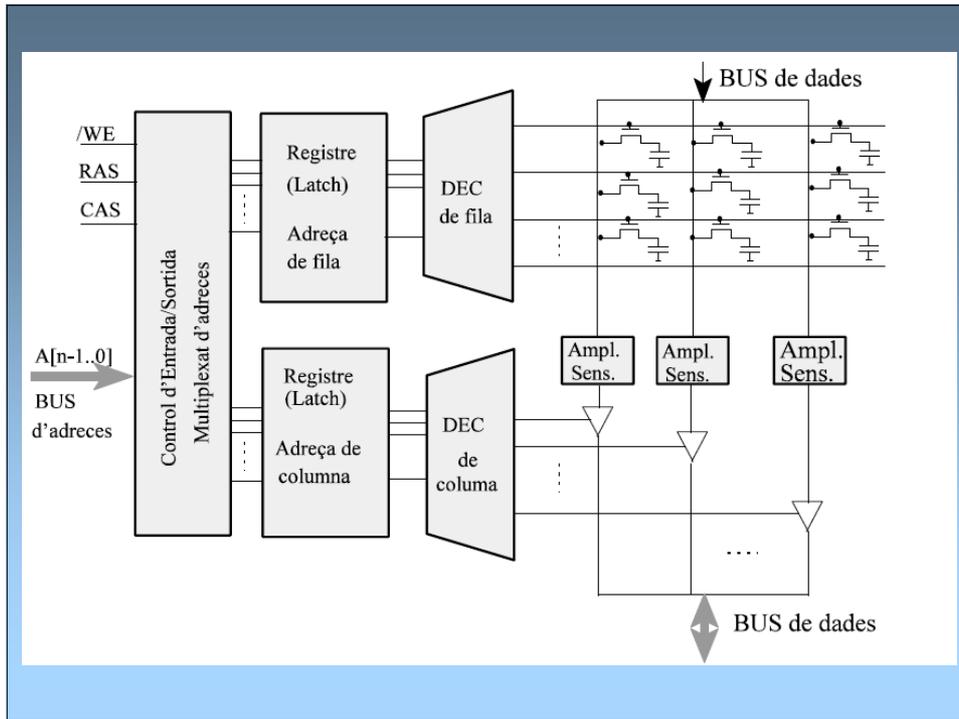


Proceso de lectura



Proceso de refresco





Memories ROM

| Posició de Memòria | Direcció $A_2 A_1 A_0$ | Contingut $D_3 D_2 D_1 D_0$ |
|--------------------|---------------------------|--------------------------------|
| m_0 | 0 0 0 | 0 1 0 0 |
| m_1 | 0 0 1 | 0 1 1 1 |
| m_2 | 0 1 0 | 1 0 1 0 |
| m_3 | 0 1 1 | 1 1 0 1 |
| m_4 | 1 0 0 | 0 0 1 0 |
| m_5 | 1 0 1 | 1 0 1 1 |
| m_6 | 1 1 0 | 0 1 1 1 |
| m_7 | 1 1 1 | 0 1 0 0 |

Memorias ROM

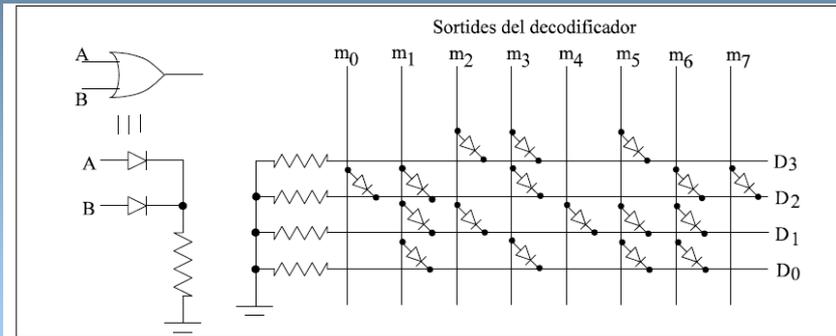


Figura 3.14

