Sistemas Electrónicos Digitales
2º Curso Ingeniería Técnica Industrial

Lógica Modular Combinacional

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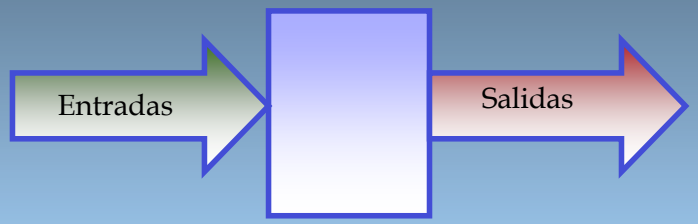
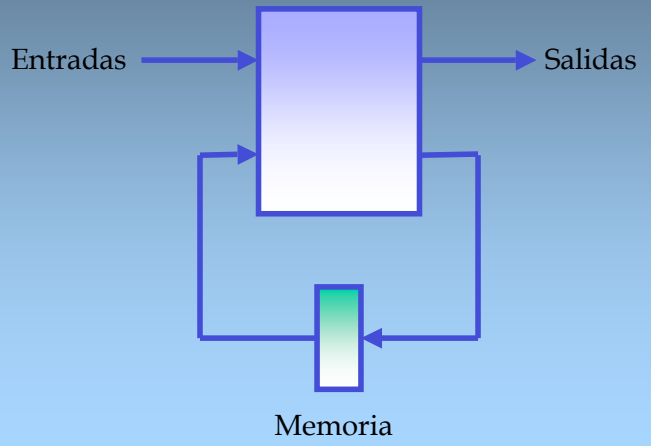
Universitat de les Illes Balears

Índice

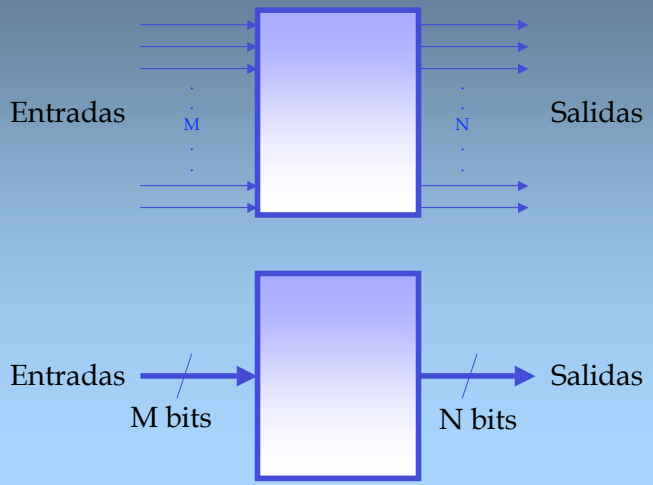
Sistema Combinacional



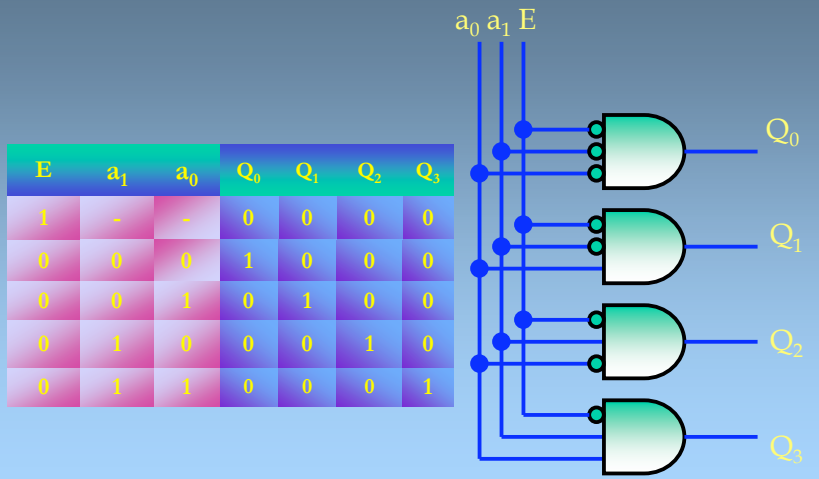
Sistema secuencial



Sistema combinacional



Decodificadores

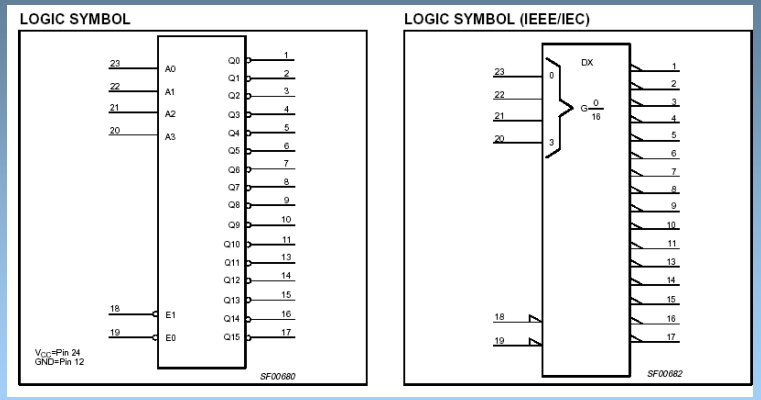


E	a_1	a_0	Q_0	Q_1	Q_2	Q_3
1	-	-	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	1	0
0	1	1	0	0	0	1

Decodificadores

- Generan los productos canónicos de las variables de entrada al sistema.
- Consisten en ‘n’ entradas y ‘2^n’ salidas
- Aplicación: Conversores de código

Decodificador MSI 74154



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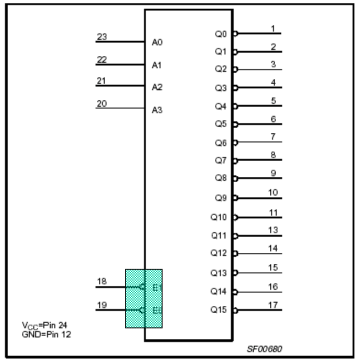

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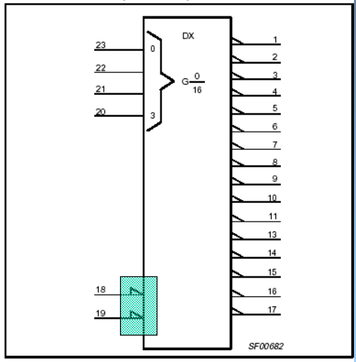

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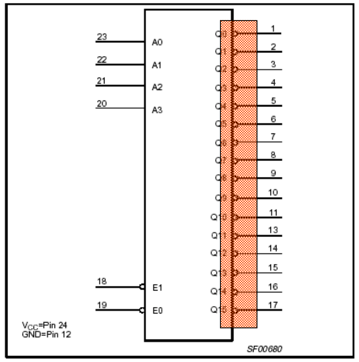

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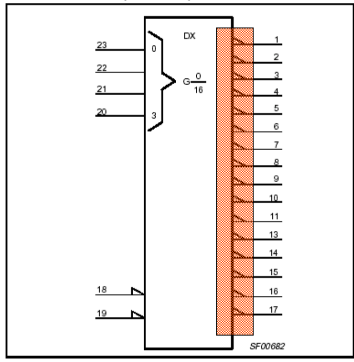

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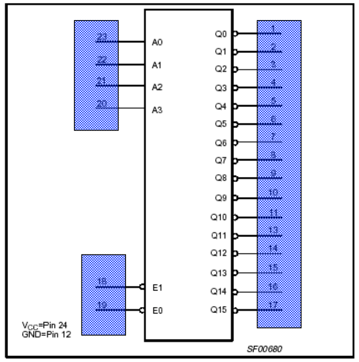

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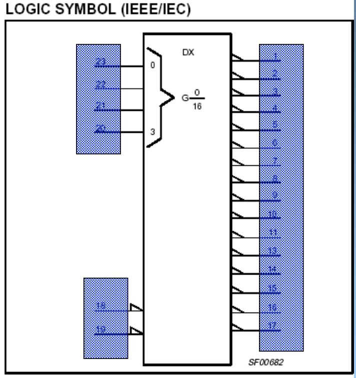

Decodificador 74154

FUNCTION TABLE

INPUTS						OUTPUTS									OUTPUTS						
$\overline{E0}$	$\overline{E1}$	A0	A1	A2	A3	$\overline{Q0}$	$\overline{Q1}$	$\overline{Q2}$	$\overline{Q3}$	$\overline{Q4}$	$\overline{Q5}$	$\overline{Q6}$	$\overline{Q7}$	$\overline{Q8}$	$\overline{Q9}$	$\overline{Q10}$	$\overline{Q11}$	$\overline{Q12}$	$\overline{Q13}$	$\overline{Q14}$	$\overline{Q15}$
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

Decodificador 74154

FUNCTION TABLE

INPUTS						OUTPUTS									OUTPUTS						
$\overline{E}_0$	$\overline{E}_1$	A0	A1	A2	A3	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$	$\overline{Q}_8$	$\overline{Q}_9$	$\overline{Q}_{10}$	$\overline{Q}_{11}$	$\overline{Q}_{12}$	$\overline{Q}_{13}$	$\overline{Q}_{14}$	$\overline{Q}_{15}$
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

Decodificador 74154

FUNCTION TABLE

INPUTS						OUTPUTS									OUTPUTS						
$\overline{E}_0$	$\overline{E}_1$	A0	A1	A2	A3	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$	$\overline{Q}_8$	$\overline{Q}_9$	$\overline{Q}_{10}$	$\overline{Q}_{11}$	$\overline{Q}_{12}$	$\overline{Q}_{13}$	$\overline{Q}_{14}$	$\overline{Q}_{15}$
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

Decodificador 74154

FUNCTION TABLE

INPUTS						OUTPUTS									OUTPUTS						
$\overline{E}_0$	$\overline{E}_1$	A0	A1	A2	A3	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$	$\overline{Q}_8$	$\overline{Q}_9$	$\overline{Q}_{10}$	$\overline{Q}_{11}$	$\overline{Q}_{12}$	$\overline{Q}_{13}$	$\overline{Q}_{14}$	$\overline{Q}_{15}$
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
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L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

Decodificador 74154

FUNCTION TABLE

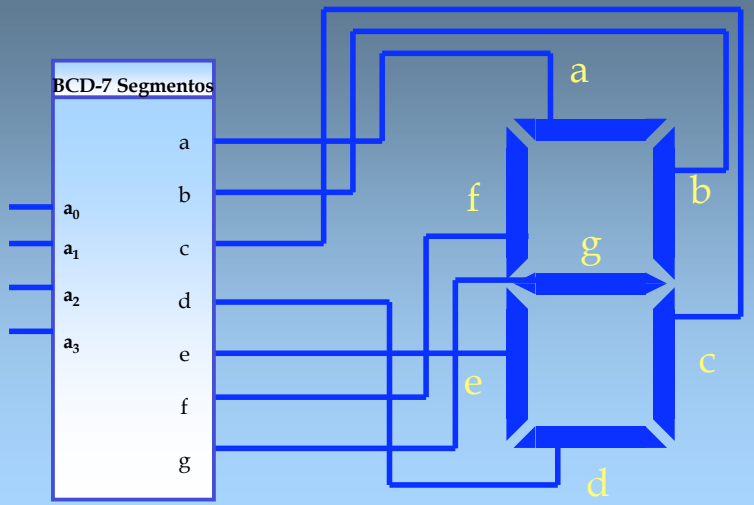
INPUTS						OUTPUTS									OUTPUTS						
$\overline{E}_0$	$\overline{E}_1$	A0	A1	A2	A3	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$	$\overline{O}_{10}$	$\overline{O}_{11}$	$\overline{O}_{12}$	$\overline{O}_{13}$	$\overline{O}_{14}$	$\overline{O}_{15}$
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

Lógica modular con decodificadores

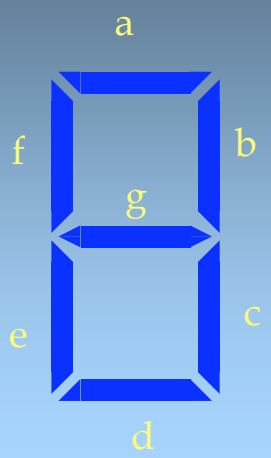
- Problema propuesto:
  - Implementar, con dos decodificadores 74154 un decodificador de 5 a 32 bits

Decodificador BCD-7 Segmentos



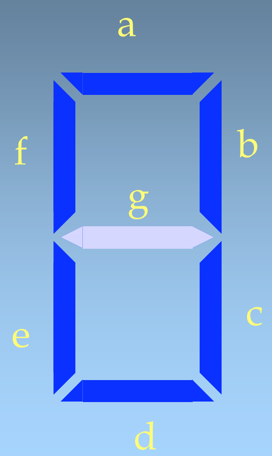
Decodificador BCD-7 Segmentos

$a_3\ a_2\ a_1\ a_0$	a	b	c	d	e	f	g
0 0 0 0	1	1	1	1	1	1	0
0 0 0 1	0	1	1	0	0	0	0
0 0 1 0	1	1	0	1	1	0	1
0 0 1 1	1	1	1	1	0	0	1
0 1 0 0	0	1	1	0	0	1	1
0 1 0 1	1	0	1	1	0	1	1
0 1 1 0	1	0	1	1	1	1	1
0 1 1 1	1	1	1	0	0	0	0
1 0 0 0	1	1	1	1	1	1	1
1 0 0 1	1	1	1	1	0	1	1



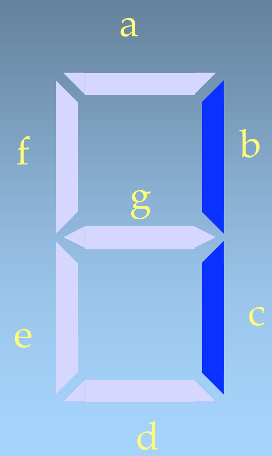
Decodificador BCD-7 Segmentos

a_3 a_2 a_1 a_0	a	b	c	d	e	f	g
0 0 0 0	1	1	1	1	1	1	0
0 0 0 1	0	1	1	0	0	0	0
0 0 1 0	1	1	0	1	1	0	1
0 0 1 1	1	1	1	1	0	0	1
0 1 0 0	0	1	1	0	0	1	1
0 1 0 1	1	0	1	1	0	1	1
0 1 1 0	1	0	1	1	1	1	1
0 1 1 1	1	1	1	0	0	0	0
1 0 0 0	1	1	1	1	1	1	1
1 0 0 1	1	1	1	1	0	1	1



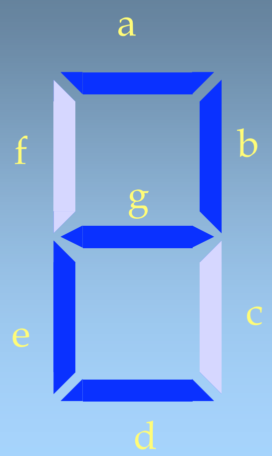
Decodificador BCD-7 Segmentos

a_3 a_2 a_1 a_0	a	b	c	d	e	f	g
0 0 0 0	1	1	1	1	1	1	0
0 0 0 1	0	1	1	0	0	0	0
0 0 1 0	1	1	0	1	1	0	1
0 0 1 1	1	1	1	1	0	0	1
0 1 0 0	0	1	1	0	0	1	1
0 1 0 1	1	0	1	1	0	1	1
0 1 1 0	1	0	1	1	1	1	1
0 1 1 1	1	1	1	0	0	0	0
1 0 0 0	1	1	1	1	1	1	1
1 0 0 1	1	1	1	1	0	1	1



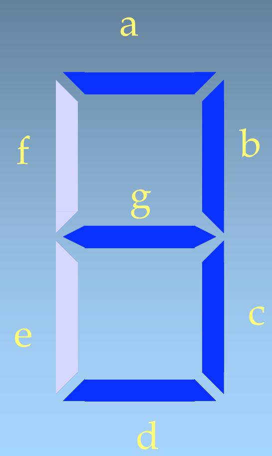
Decodificador BCD-7 Segmentos

a_3 a_2 a_1 a_0	a	b	c	d	e	f	g
0 0 0 0	1	1	1	1	1	1	0
0 0 0 1	0	1	1	0	0	0	0
0 0 1 0	1	1	0	1	1	0	1
0 0 1 1	1	1	1	1	0	0	1
0 1 0 0	0	1	1	0	0	1	1
0 1 0 1	1	0	1	1	0	1	1
0 1 1 0	1	0	1	1	1	1	1
0 1 1 1	1	1	1	0	0	0	0
1 0 0 0	1	1	1	1	1	1	1
1 0 0 1	1	1	1	1	0	1	1



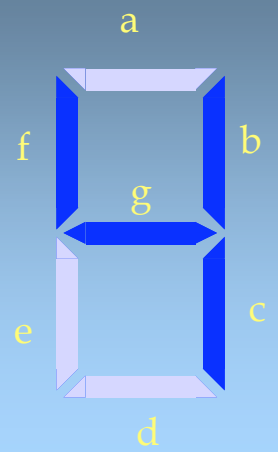
Decodificador BCD-7 Segmentos

a_3 a_2 a_1 a_0	a	b	c	d	e	f	g
0 0 0 0	1	1	1	1	1	1	0
0 0 0 1	0	1	1	0	0	0	0
0 0 1 0	1	1	0	1	1	0	1
0 0 1 1	1	1	1	1	0	0	1
0 1 0 0	0	1	1	0	0	1	1
0 1 0 1	1	0	1	1	0	1	1
0 1 1 0	1	0	1	1	1	1	1
0 1 1 1	1	1	1	0	0	0	0
1 0 0 0	1	1	1	1	1	1	1
1 0 0 1	1	1	1	1	0	1	1



Decodificador BCD-7 Segmentos

$a_3\ a_2\ a_1\ a_0$	a	b	c	d	e	f	g
0 0 0 0	1	1	1	1	1	1	0
0 0 0 1	0	1	1	0	0	0	0
0 0 1 0	1	1	0	1	1	0	1
0 0 1 1	1	1	1	1	0	0	1
0 1 0 0	0	1	1	0	0	1	1
0 1 0 1	1	0	1	1	0	1	1
0 1 1 0	1	0	1	1	1	1	1
0 1 1 1	1	1	1	0	0	0	0
1 0 0 0	1	1	1	1	1	1	1
1 0 0 1	1	1	1	1	0	1	1

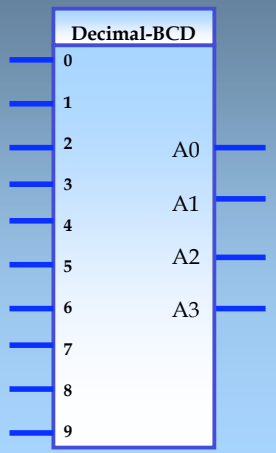


Codificadores

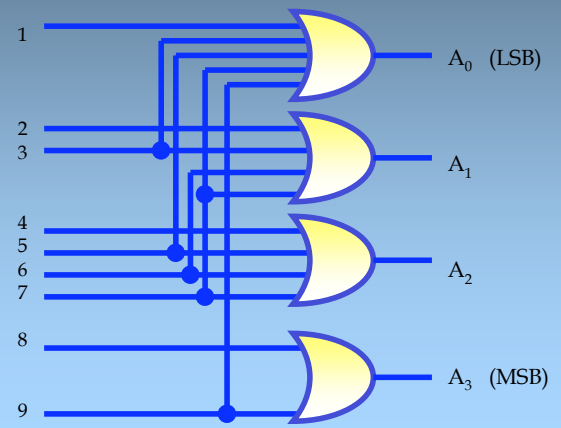
- Realizan la función inversa al decodificador
  - Ej: Codificación de un teclado
  - Codificador con prioridad
  - Codificador Decimal-BCD
  - Codificador Octal-Binario

Conversor Decimal-BCD

Digito	A_3	A_2	A_1	A_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

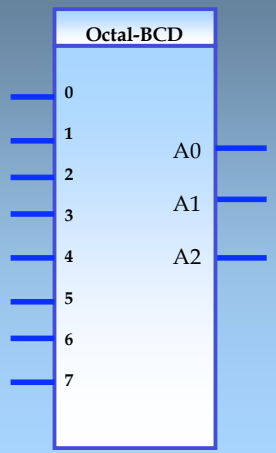


Conversor Decimal-BCD

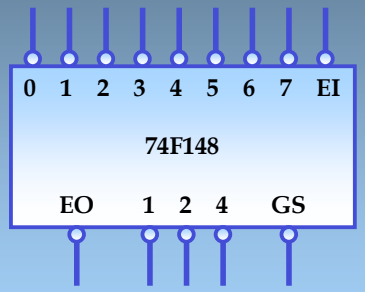


Conversor Octal-Binario

Digito	A_2	A_1	A_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1



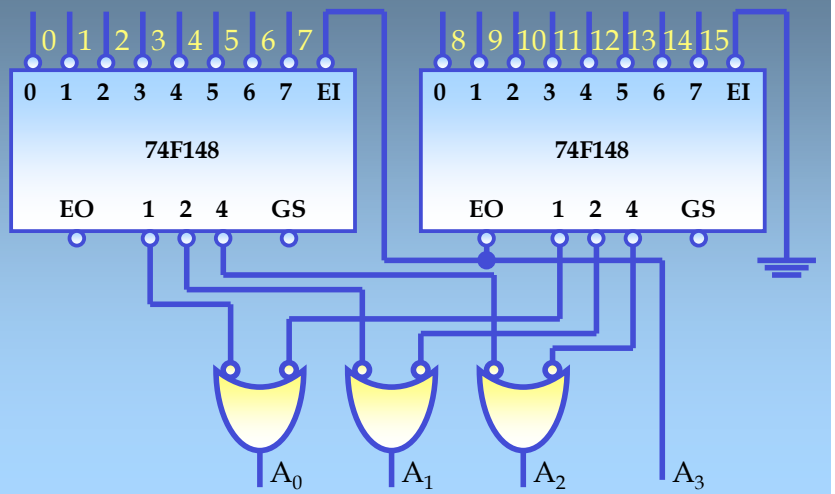
Conversor MSI 74x148



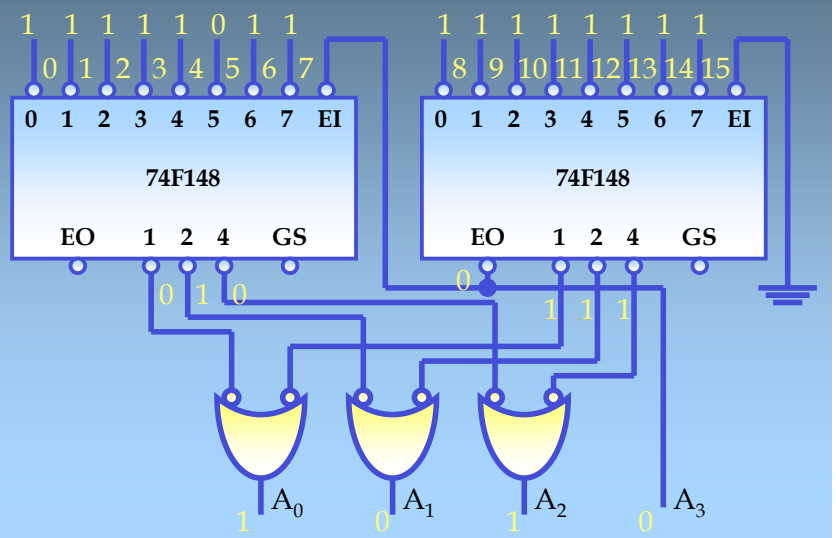
Conversor de MSI 74x148

EI	0 1 2 3 4 5 6 7	EO	GS	4	2	1
1	- - - - - - - -	1	1	1	1	1
0	1 1 1 1 1 1 1 1	0	1	1	1	1
0	0 1 1 1 1 1 1 1	1	0	1	1	1
0	- 0 1 1 1 1 1 1	1	0	1	1	0
0	- - 0 1 1 1 1 1	1	0	1	0	1
0	- - - 0 1 1 1 1	1	0	1	0	0
0	- - - - 0 1 1 1	1	0	0	1	1
0	- - - - - 0 1 1	1	0	0	1	0
0	- - - - - - 0 1	1	0	0	0	1
0	- - - - - - - 0	1	0	0	0	0

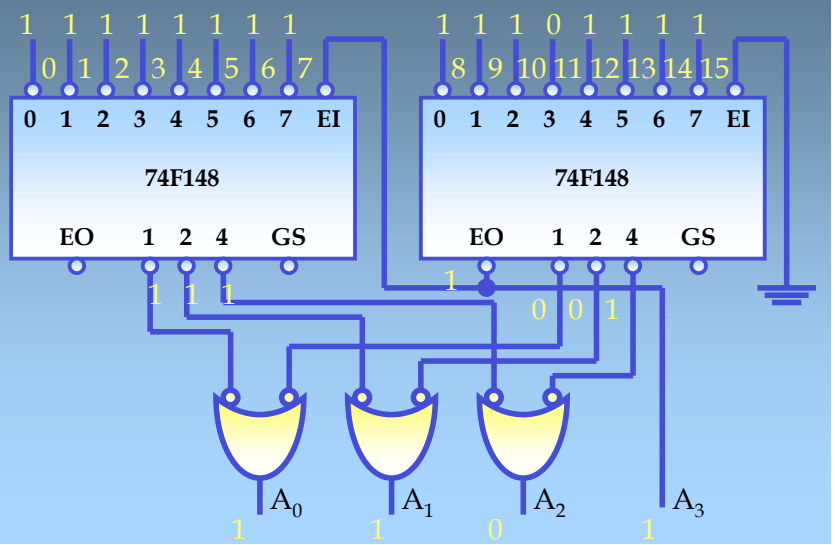
Conversor de 16 a 4 líneas



Conversor de 16 a 4 líneas

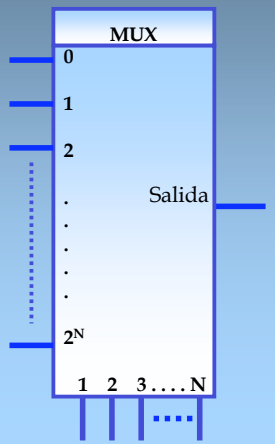


Conversor de 16 a 4 líneas



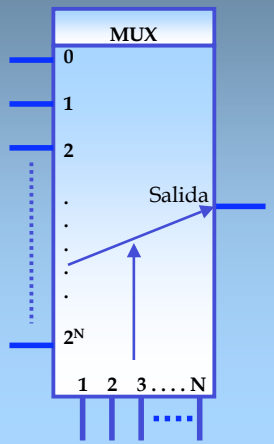
Multiplexores

- 2^N canales de entrada, un canal de salida, N bits de control

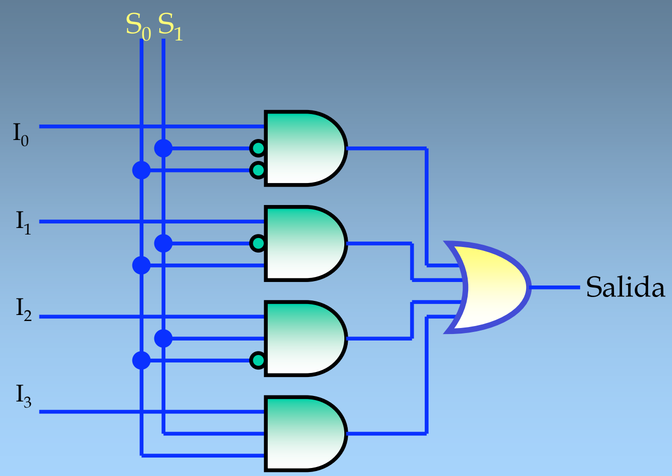


Multiplexores

- 2^N canales de entrada, un canal de salida, N bits de control

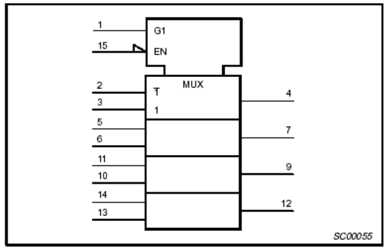


Multiplexor de 4 entradas de 1 bit

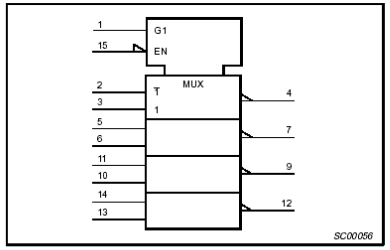


Multiplexor 74157 74158

IEC/IEEE SYMBOL – 74ALS157



IEC/IEEE SYMBOL – 74ALS158



FUNCTION TABLE – 74ALS157

INPUTS				OUTPUTS
$\overline{E}$	S	I0n	I1n	Yn
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High voltage level
L = Low voltage level
X = Don't care

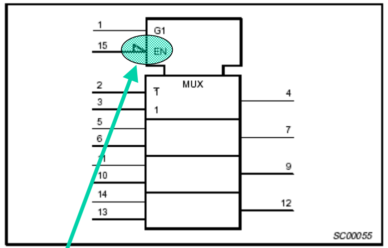
FUNCTION TABLE – 74ALS158

INPUTS				OUTPUTS
$\overline{E}$	S	I0n	I1n	$\overline{Yn}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

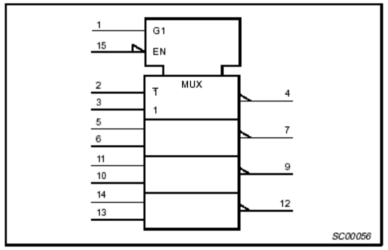
H = High voltage level
L = Low voltage level
X = Don't care

Multiplexor 74157 74158

IEC/IEEE SYMBOL – 74ALS157



IEC/IEEE SYMBOL – 74ALS158



FUNCTION TABLE – 74ALS157

INPUTS				OUTPUTS
$\overline{E}$	S	I0n	I1n	Yn
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High voltage level
L = Low voltage level
X = Don't care

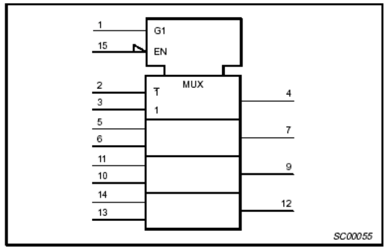
FUNCTION TABLE – 74ALS158

INPUTS				OUTPUTS
$\overline{E}$	S	I0n	I1n	$\overline{Yn}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

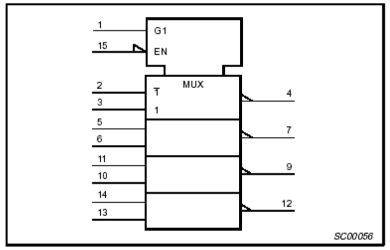
H = High voltage level
L = Low voltage level
X = Don't care

Multiplexor 74157 74158

IEC/IEEE SYMBOL – 74ALS157



IEC/IEEE SYMBOL – 74ALS158



FUNCTION TABLE – 74ALS157

INPUTS				OUTPUTS
$\overline{E}$	S	I0n	I1n	Yn
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High voltage level
L = Low voltage level
X = Don't care

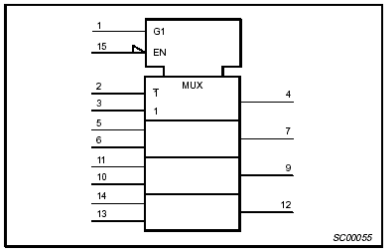
FUNCTION TABLE – 74ALS158

INPUTS				OUTPUTS
$\overline{E}$	S	I0n	I1n	$\overline{Yn}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

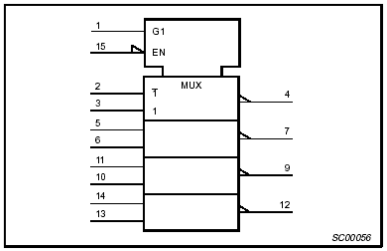
H = High voltage level
L = Low voltage level
X = Don't care

Multiplexor 74157 74158

IEC/IEEE SYMBOL – 74ALS157



IEC/IEEE SYMBOL – 74ALS158



FUNCTION TABLE – 74ALS157

INPUTS				OUTPUTS
$\overline{E}$	S	I0n	I1n	Yn
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High voltage level
L = Low voltage level
X = Don't care

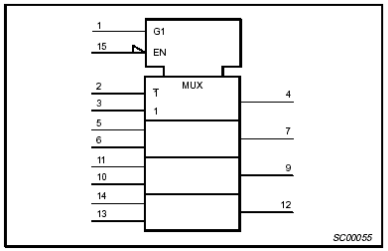
FUNCTION TABLE – 74ALS158

INPUTS				OUTPUTS
$\overline{E}$	S	I0n	I1n	$\overline{Y}$n
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

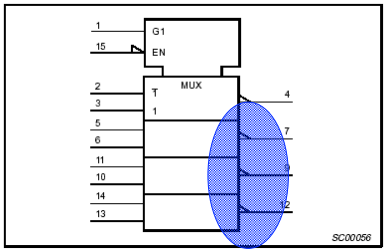
H = High voltage level
L = Low voltage level
X = Don't care

Multiplexor 74157 74158

IEC/IEEE SYMBOL – 74ALS157



IEC/IEEE SYMBOL – 74ALS158



FUNCTION TABLE – 74ALS157

INPUTS				OUTPUTS
$\overline{E}$	S	I0n	I1n	Yn
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE – 74ALS158

INPUTS				OUTPUTS
$\overline{E}$	S	I0n	I1n	$\overline{Y}$n
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care

Implementación de funciones

- Salida=Σ_i (I_i m_i EN)

- Por tanto se puede implementar cualquier función lógica F=Σ_i (f_i m_i)

Implementación de funciones

- Salida=Σ_i (I_i m_i EN)

Entrada 'i'

- Por tanto se puede implementar cualquier función lógica F=Σ_i (f_i m_i)

Implementación de funciones

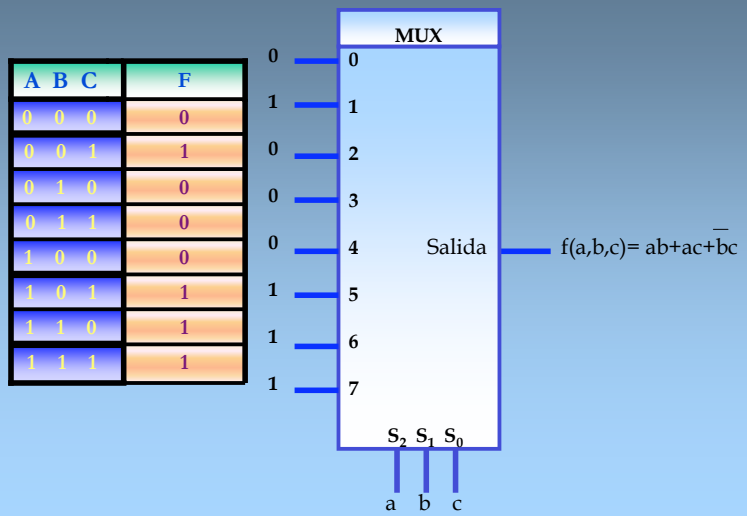
- Salida=Σ_i (I_i m_i EN)

Mintérmino de control

Entrada 'i'

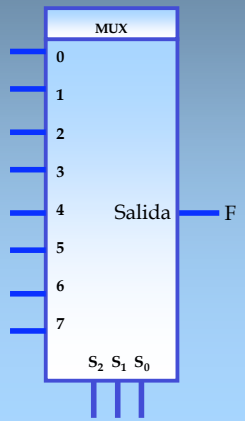
- Por tanto se puede implementar cualquier función lógica F=Σ_i (f_i m_i)

Ejemplo de implementación

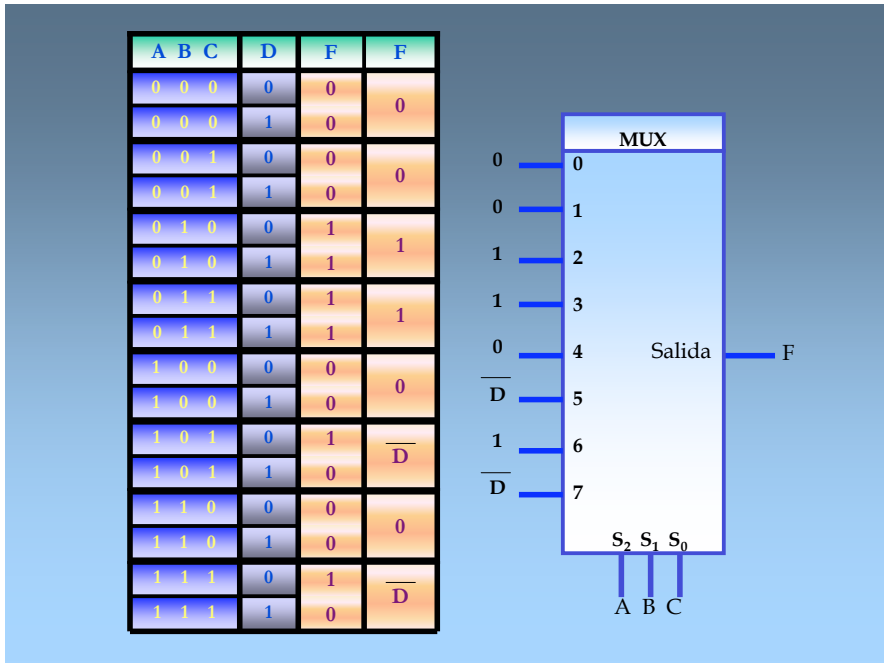


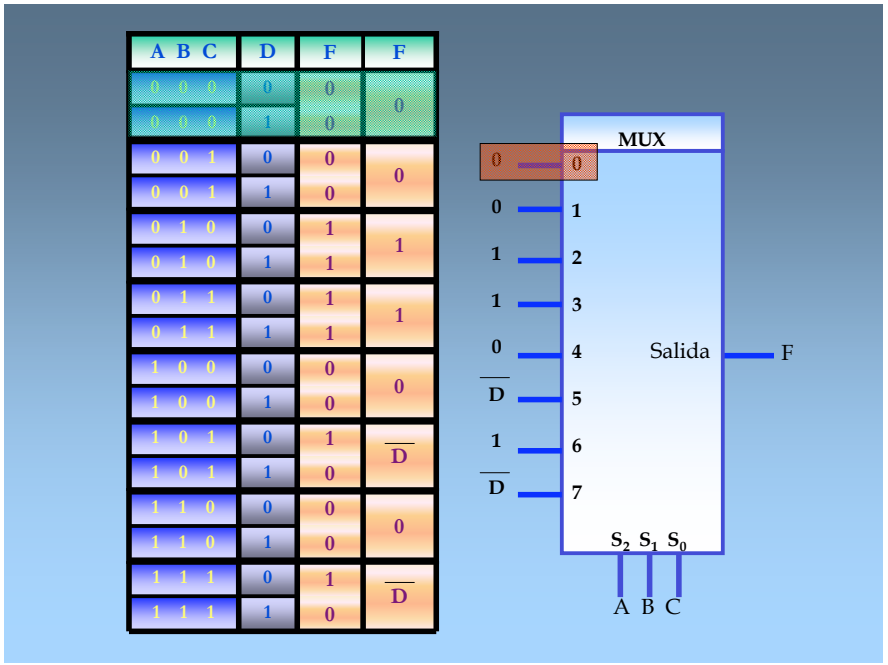
Implementación funciones de 4 variables

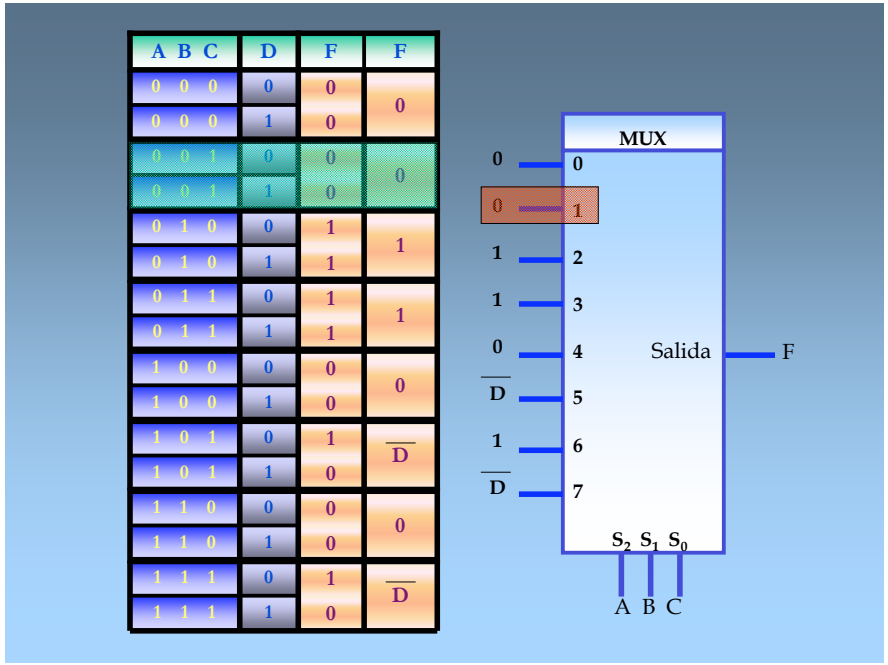
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

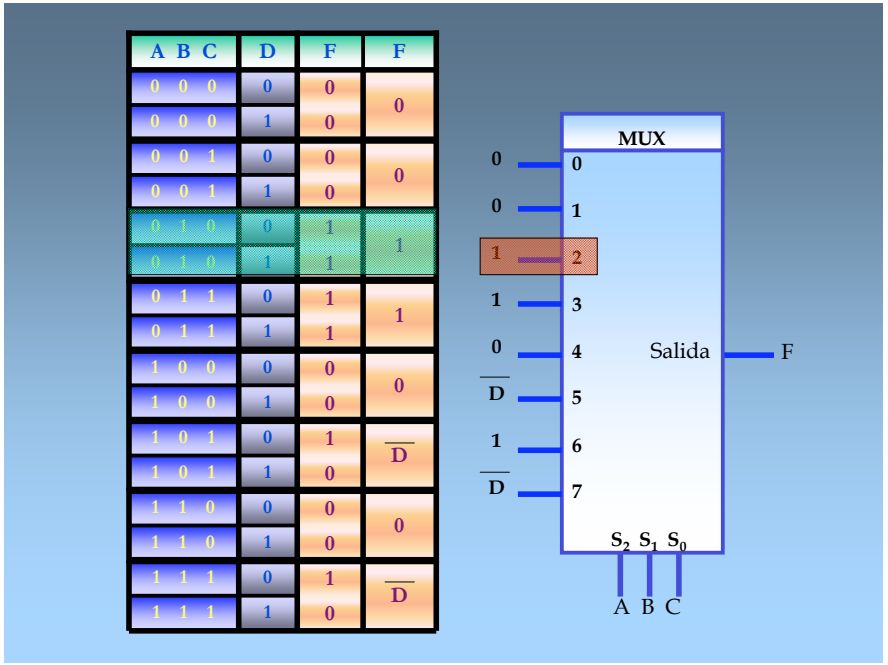


A	B	C	D	F	F
0	0	0	0	0	0
0	0	0	1	0	
0	0	1	0	0	0
0	0	1	1	0	
0	1	0	0	1	1
0	1	0	1	1	
0	1	1	0	1	1
0	1	1	1	1	
1	0	0	0	0	0
1	0	0	1	0	
1	0	1	0	1	$\overline{D}$
1	0	1	1	0	
1	1	0	0	0	0
1	1	0	1	0	
1	1	1	0	1	$\overline{D}$
1	1	1	1	0	

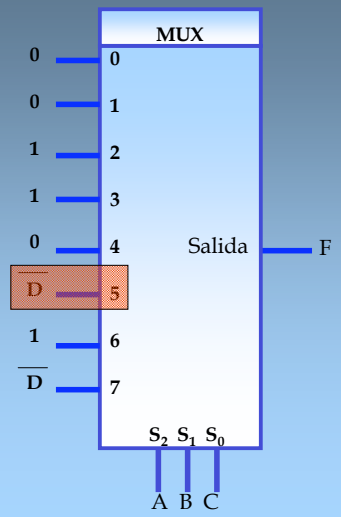

A B C
D
F
F
MUX
Salida
F
S_2 S_1 S_0
A B C


A B C
D
F
F
MUX
Salida
F
S_2 S_1 S_0
A B C


A B C
D
F
F
MUX
Salida
F
S_2 S_1 S_0
A B C


A B C
D
F
F
MUX
Salida
F
S_2 S_1 S_0
A B C

A B C	D	F	F
0 0 0	0	0	0
0 0 0	1	0	
0 0 1	0	0	0
0 0 1	1	0	
0 1 0	0	1	1
0 1 0	1	1	
0 1 1	0	1	1
0 1 1	1	1	
1 0 0	0	0	0
1 0 0	1	0	
1 0 1	0	1	$\overline{D}$
1 0 1	1	0	
1 1 0	0	0	0
1 1 0	1	0	
1 1 1	0	1	$\overline{D}$
1 1 1	1	0	



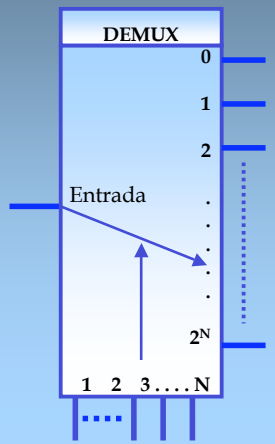
A B C D	F
0 0 0 0	0
0 0 0 1	0
0 0 1 0	0
0 0 1 1	0
0 1 0 0	1
0 1 0 1	1
0 1 1 0	1
0 1 1 1	1
1 0 0 0	0
1 0 0 1	0
1 0 1 0	1
1 0 1 1	0
1 1 0 0	0
1 1 0 1	0
1 1 1 0	1
1 1 1 1	0

Ejercicio

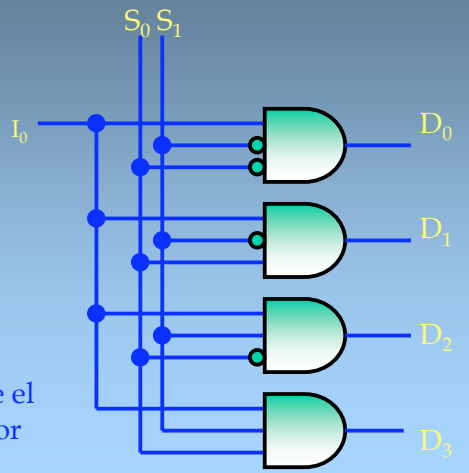
Implementar la función F a partir de un multiplexor de 4 bits y de la lógica necesaria

Demultiplexores

- Un canal de entrada, 2^N canales de salida, N bits de control

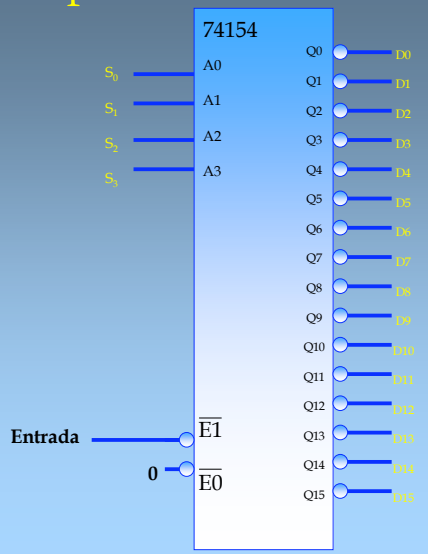


Demultiplexor de 1 línea a 4 líneas

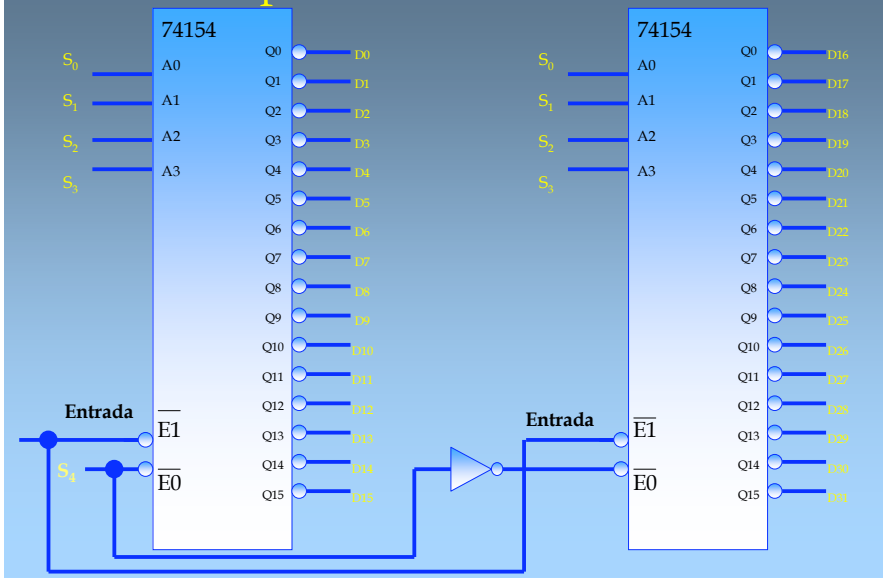


Idéntico que el decodificador de 2 a 4

Demultiplexor utilizando el 74154

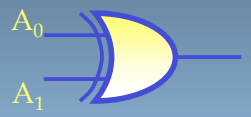


Demultiplexor utilizando el 74154



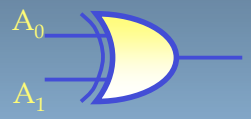
Generador/Comprobador de paridad

Generador/Comprobador de paridad



X es 1 si el número de 'unos' es impar

Generador/Comprobador de paridad

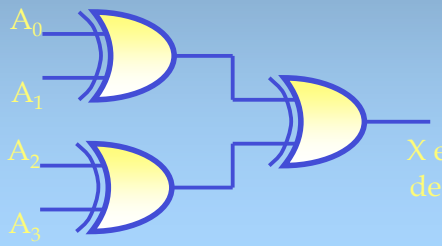


X es 1 si el número de 'unos' es impar

A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

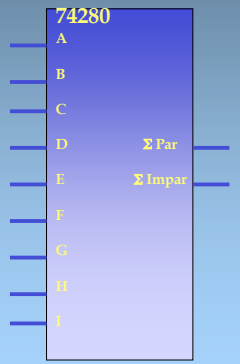
Generador/Comprobador de paridad

X es 1 si el número de 'unos' es impar



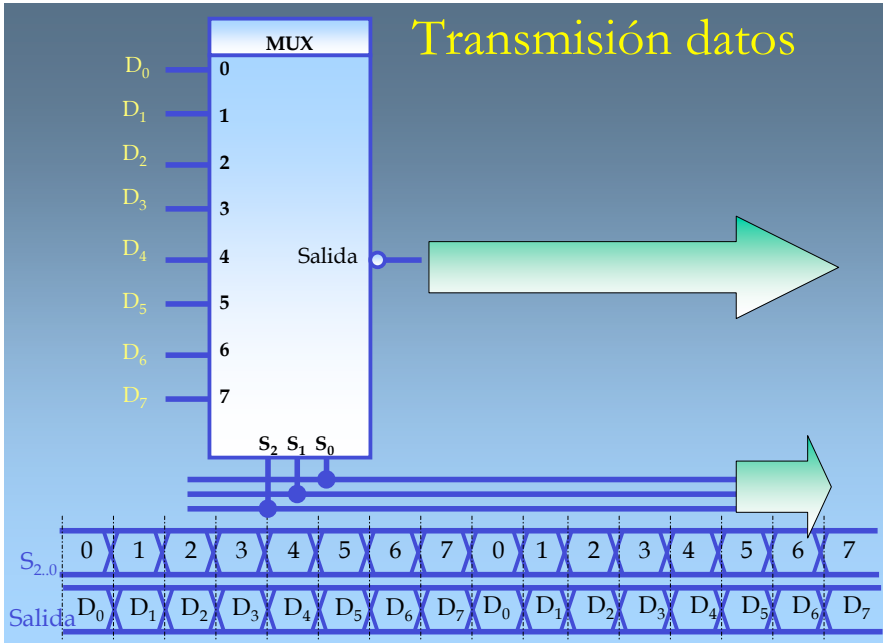
X es 1 si el número de 'unos' es impar

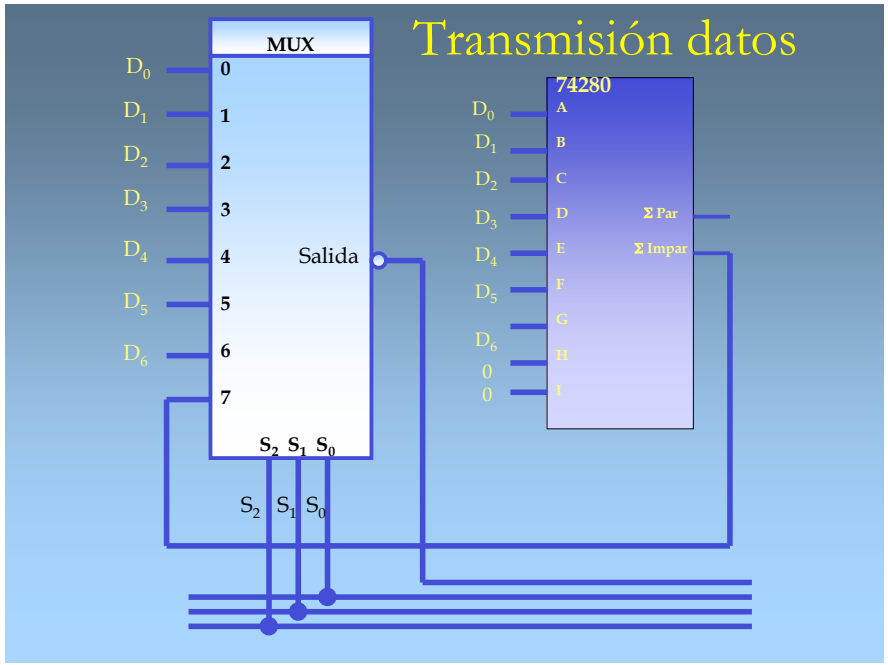
Generador/Comprobador de paridad 74280

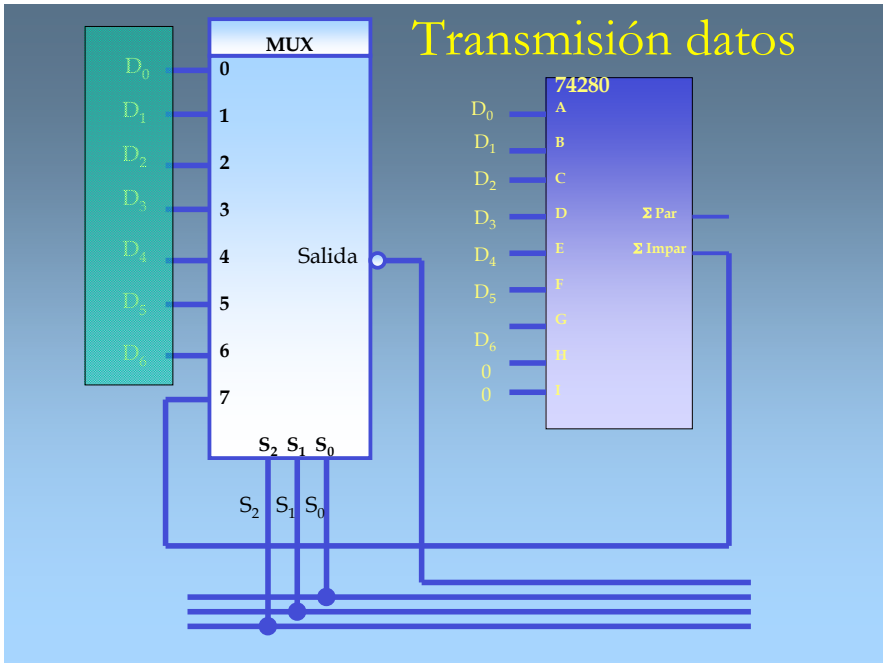


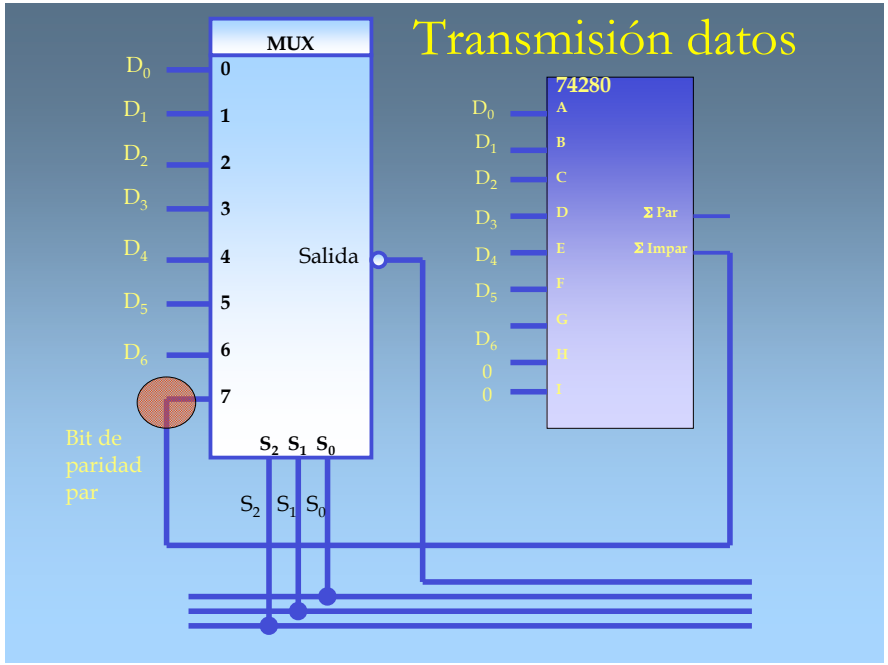
Número de entradas en nivel ALTO	Salidas	
	Σ Par	Σ Impar
0, 2, 4, 6, 8	1	0
1, 3, 5, 7, 9	0	1

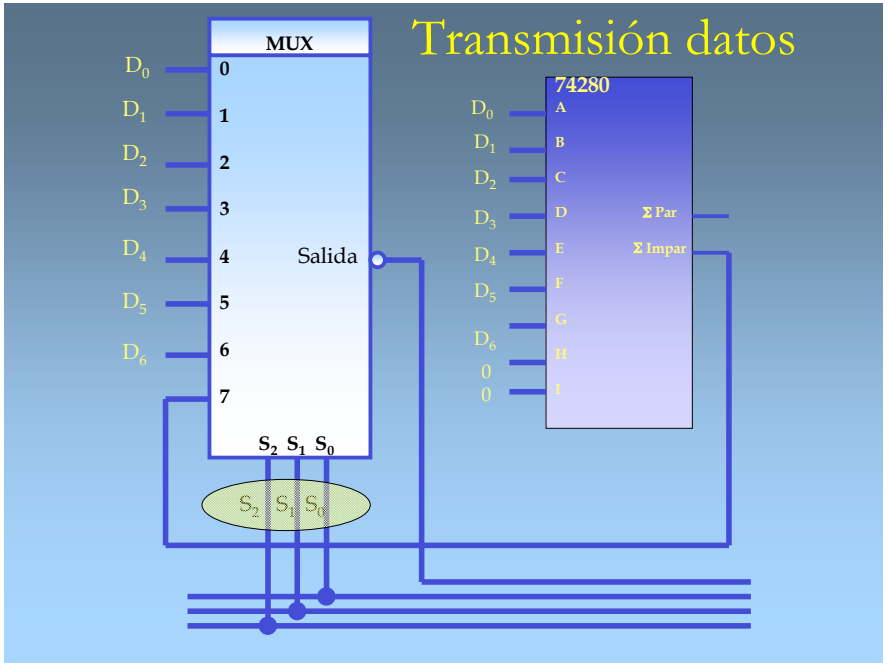
Transmisión datos

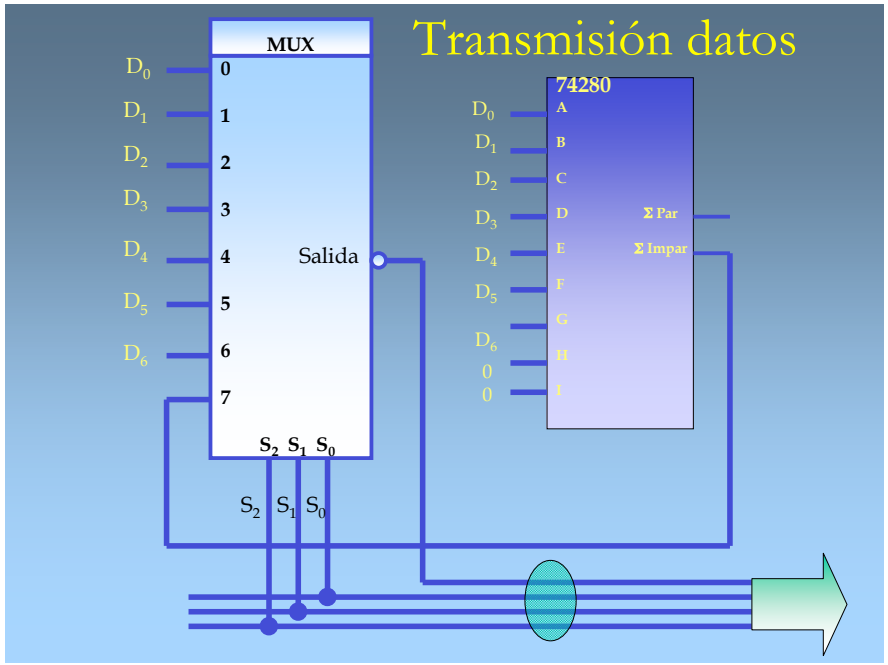


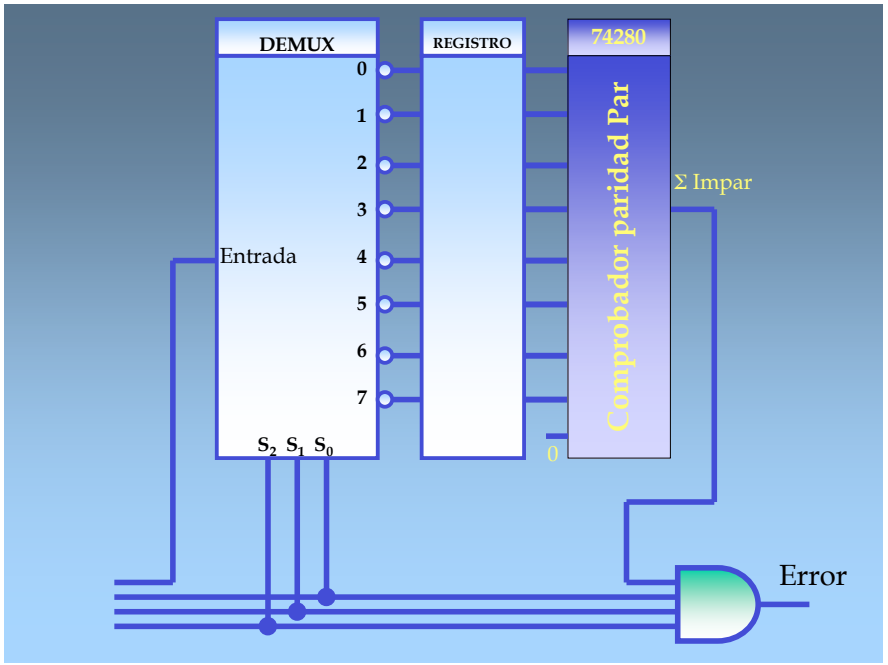

Transmisión datos
MUX
Salida
74280
Σ Par
Σ Impar

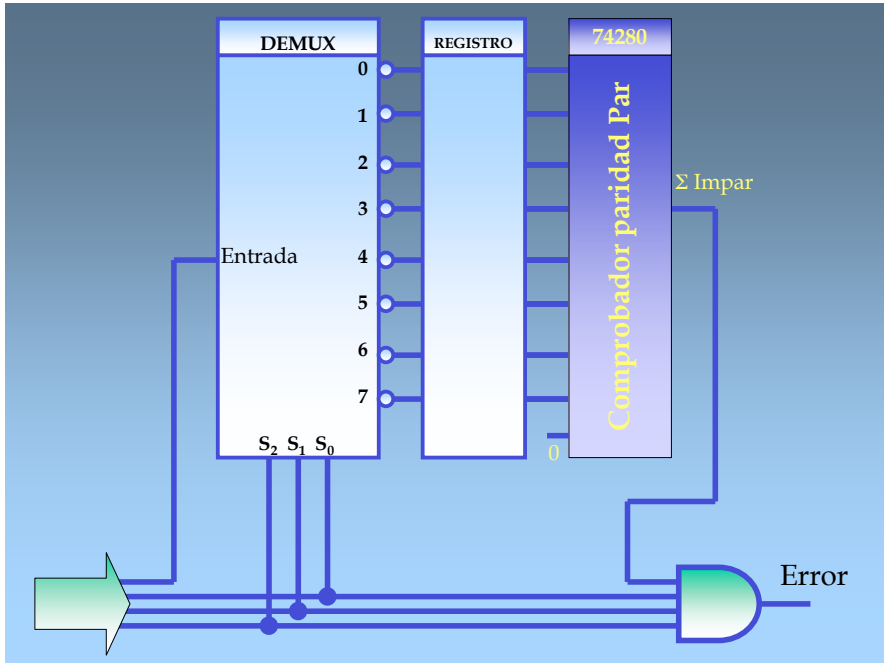

Transmisión datos
MUX
Salida
74280
Σ Par
Σ Impar

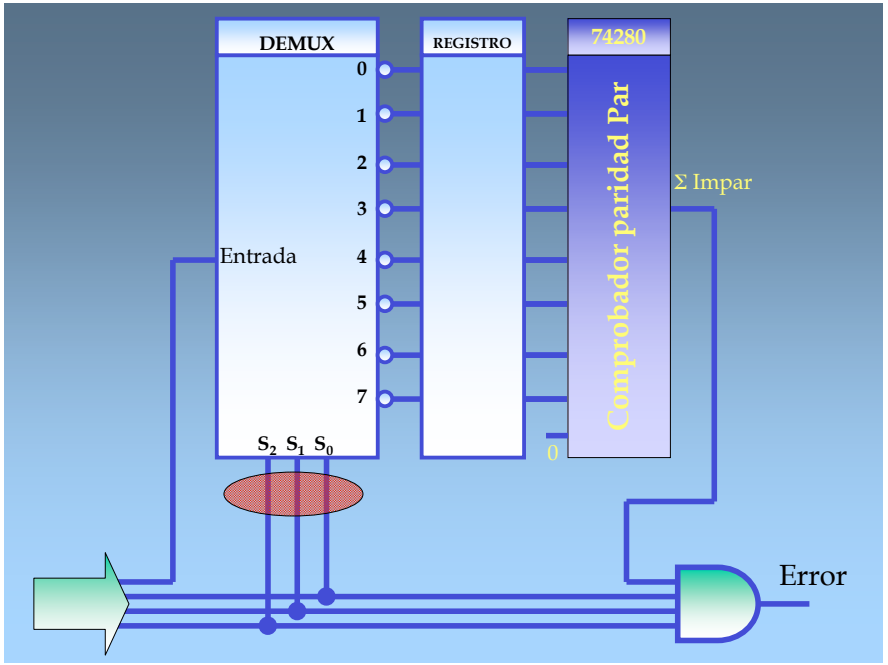

Transmisión datos
MUX
Salida
74280
Σ Par
Σ Impar
Bit de paridad par

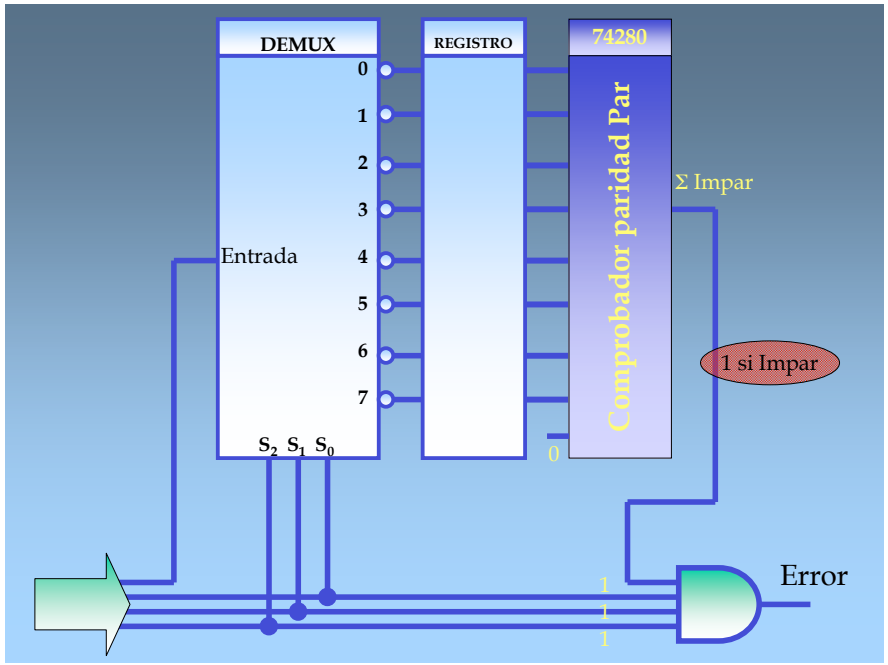

Transmisión datos
MUX
Salida
74280
Σ Par
Σ Impar


Transmisión datos
MUX
D0
D1
D2
D3
D4
D5
D6
0
1
2
3
4
5
6
7
Salida
S2 S1 S0
74280
A
B
C
D
E
F
G
H
I
Σ Par
Σ Impar


DEMUX
REGISTRO
74280
Comprobador paridad Par
Entrada
S2 S1 S0
Σ Impar
Error


DEMUX
REGISTRO
74280
Comprobador paridad Par
Entrada
S2 S1 S0
Σ Impar
Error

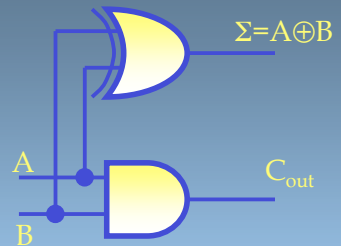

DEMUX
REGISTRO
74280
Comprobador paridad Par
Entrada
S2 S1 S0
Σ Impar
Error



Sumadores básicos

Semisumador

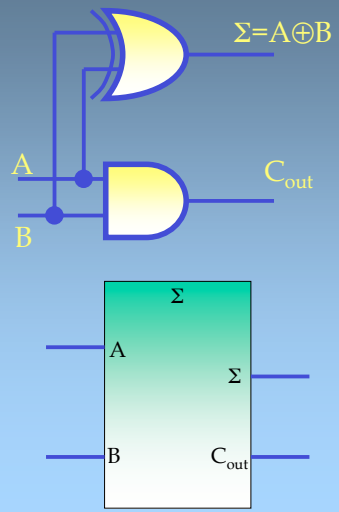
A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



Sumadores básicos

Semisumador

A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

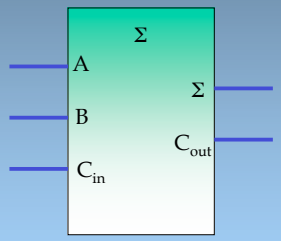


Sumador completo

C_{in}	A	B	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Sumador completo

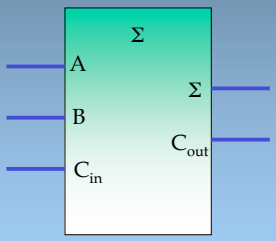
C_{in}	A	B	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



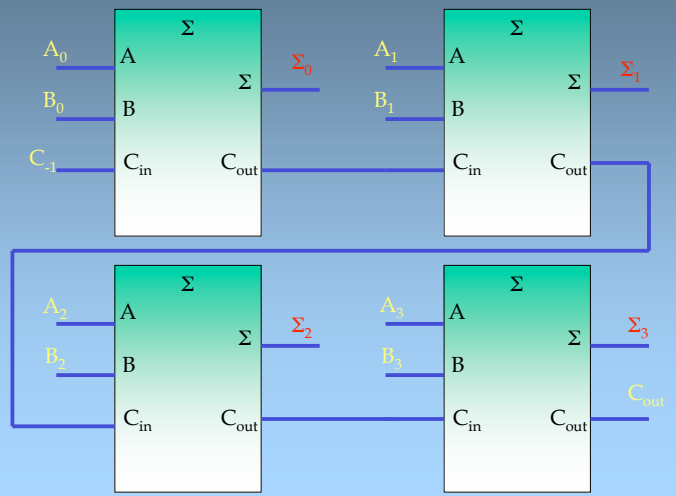
Ejercicio: Implementa un sumador completo a partir de dos semisumadores y una puerta OR

Sumador completo

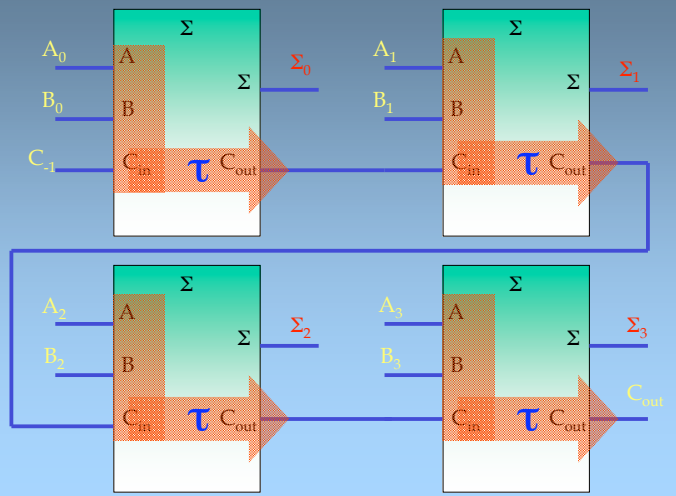
C_{in}	A	B	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



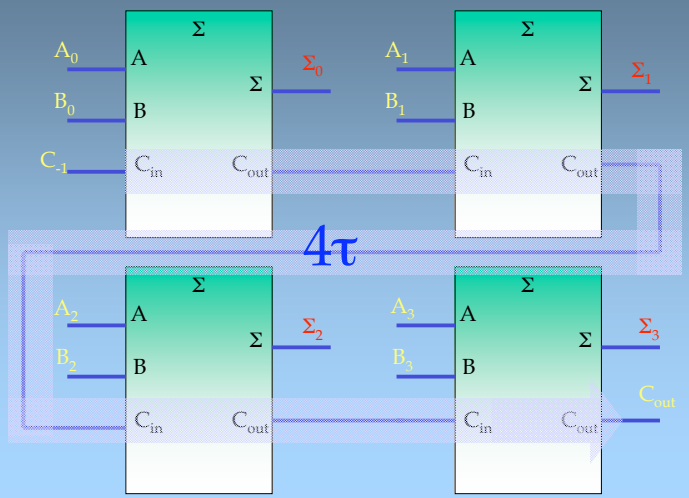
Sumador de 4 bits (propag. acarreo)



Sumador de 4 bits (propag. acarreo)

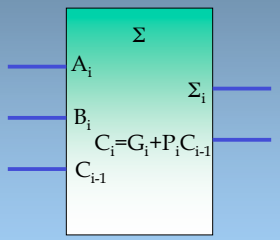


Sumador de 4 bits (propag. acarreo)



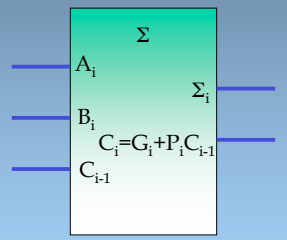
Acarreo de grupo hacia adelante

Acarreo de grupo hacia adelante



Acarreo de grupo hacia adelante

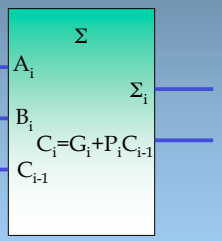
$A_{3..0} + B_{3..0} = \Sigma_{3..0}$



Acarreo de grupo hacia adelante

$$A_{3..0} + B_{3..0} = \Sigma_{3..0}$$

$C_0 = A_0 \cdot B_0 + (A_0 + B_0) \cdot C_{-1}$

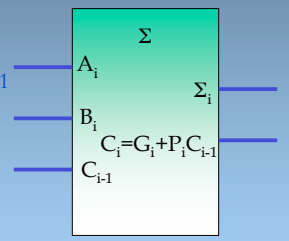


Acarreo de grupo hacia adelante

$$A_{3..0} + B_{3..0} = \Sigma_{3..0}$$

$C_0 = A_0 \cdot B_0 + (A_0 + B_0) \cdot C_{-1}$

⇓ ⇓ ⇓



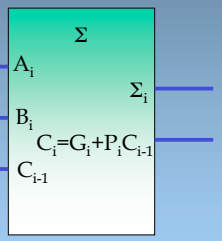
Acarreo de grupo hacia adelante

$$A_{3..0} + B_{3..0} = \Sigma_{3..0}$$

$C_0 = A_0 \cdot B_0 + (A_0 + B_0) \cdot C_{-1}$

⇓ ⇓ ⇓

$C_0 = G_0 + P_0 C_{-1}$



Acarreo de grupo hacia adelante

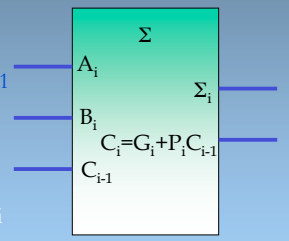
$$A_{3..0} + B_{3..0} = \Sigma_{3..0}$$

$C_0 = A_0 \cdot B_0 + (A_0 + B_0) \cdot C_{-1}$

⇓ ⇓ ⇓

$C_0 = G_0 + P_0 C_{-1}$

$P_i = A_i + B_i \quad G_i = A_i \cdot B_i$



Acarreo de grupo hacia adelante

$$A_{3..0} + B_{3..0} = \Sigma_{3..0}$$

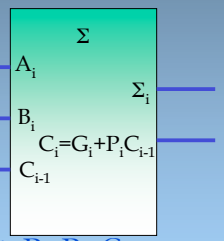
$C_0 = A_0 \cdot B_0 + (A_0 + B_0) \cdot C_{-1}$

$\Downarrow \quad \Downarrow \qquad \Downarrow$

$C_0 = G_0 + P_0 C_{-1}$

$P_i = A_i + B_i \qquad G_i = A_i \cdot B_i$

$C_1 = G_1 + P_1 \cdot C_0 = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_{-1}$



Acarreo de grupo hacia adelante

$$A_{3..0} + B_{3..0} = \Sigma_{3..0}$$

$C_0 = A_0 \cdot B_0 + (A_0 + B_0) \cdot C_{-1}$

$\Downarrow \quad \Downarrow \qquad \Downarrow$

$C_0 = G_0 + P_0 C_{-1}$

$P_i = A_i + B_i \qquad G_i = A_i \cdot B_i$

$C_1 = G_1 + P_1 \cdot C_0 = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_{-1}$

$C_2 = G_2 + P_2 \cdot C_1 = G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_{-1}$

Acarreo de grupo hacia adelante

$$A_{3..0} + B_{3..0} = \Sigma_{3..0}$$

$C_0 = A_0 \cdot B_0 + (A_0 + B_0) \cdot C_{-1}$

$\Downarrow \quad \Downarrow \qquad \Downarrow$

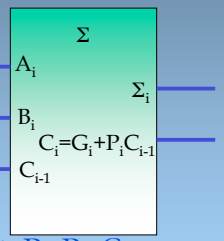
$C_0 = G_0 + P_0 C_{-1}$

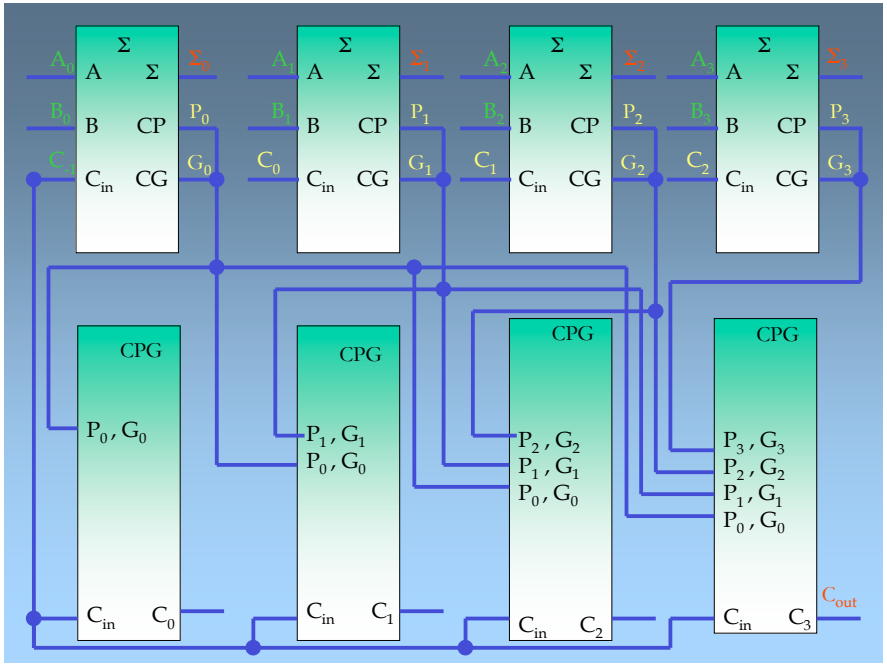
$P_i = A_i + B_i \qquad G_i = A_i \cdot B_i$

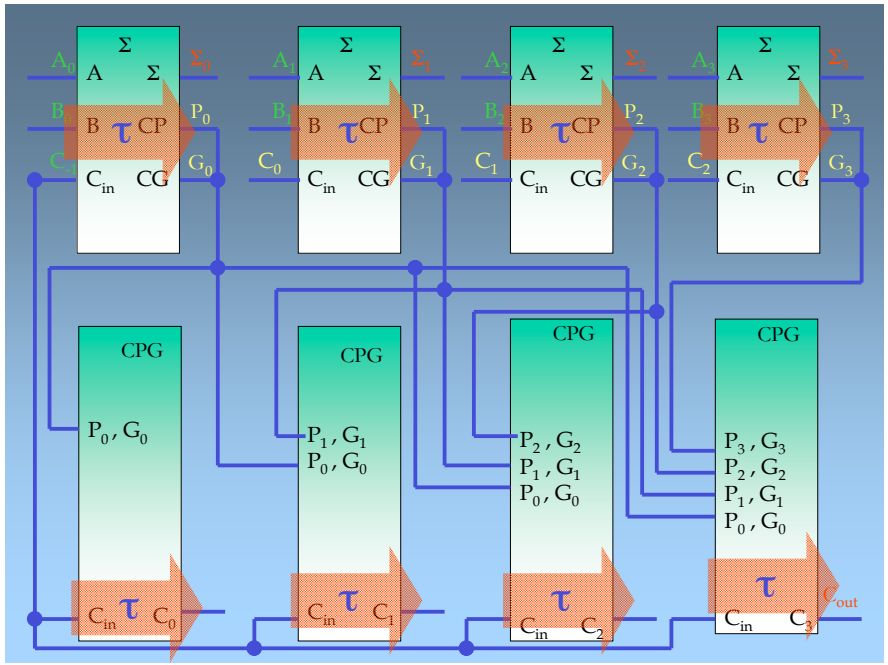
$C_1 = G_1 + P_1 \cdot C_0 = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_{-1}$

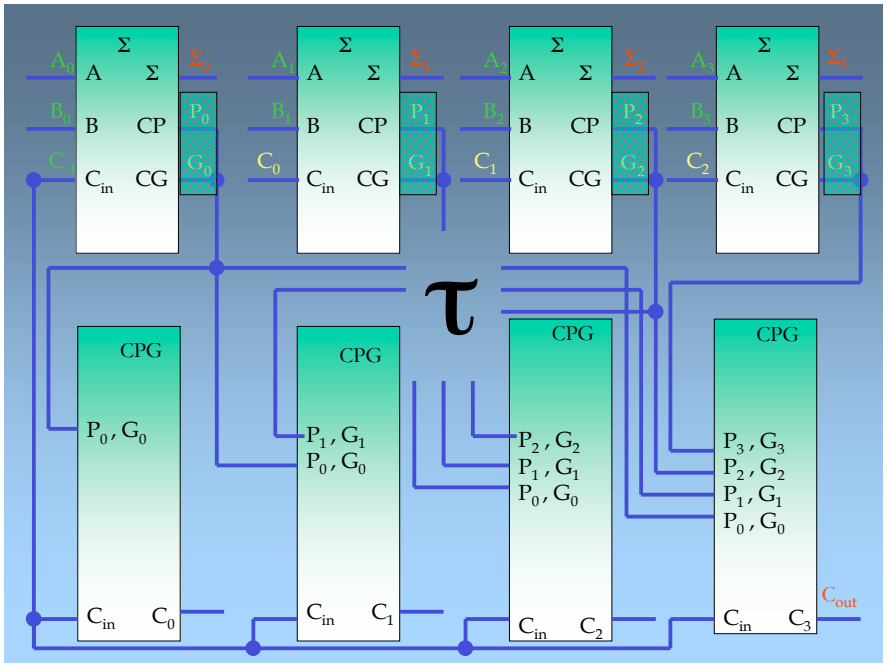
$C_2 = G_2 + P_2 \cdot C_1 = G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_{-1}$

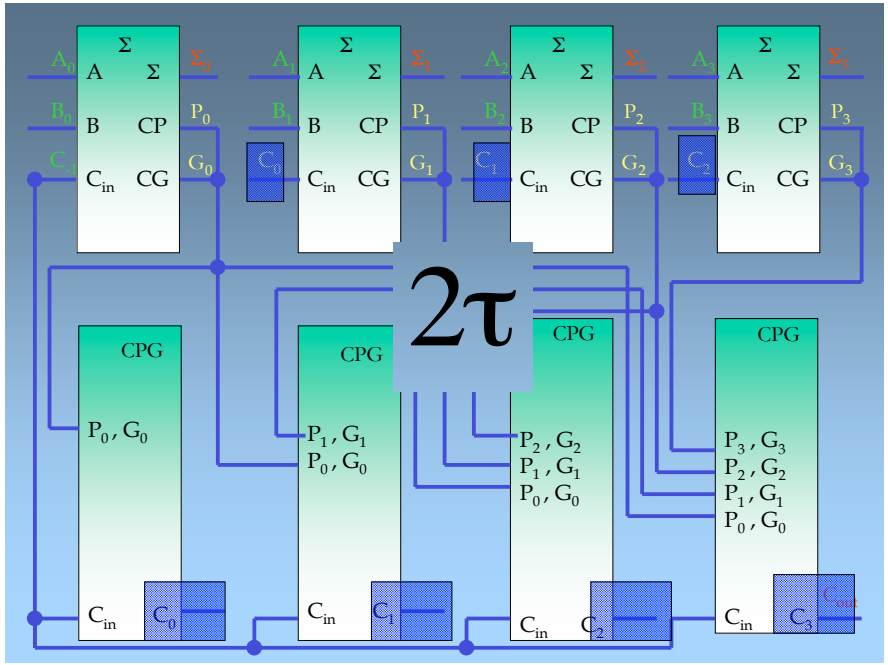
$C_3 = G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot P_1 \cdot P_0 \cdot C_{-1}$

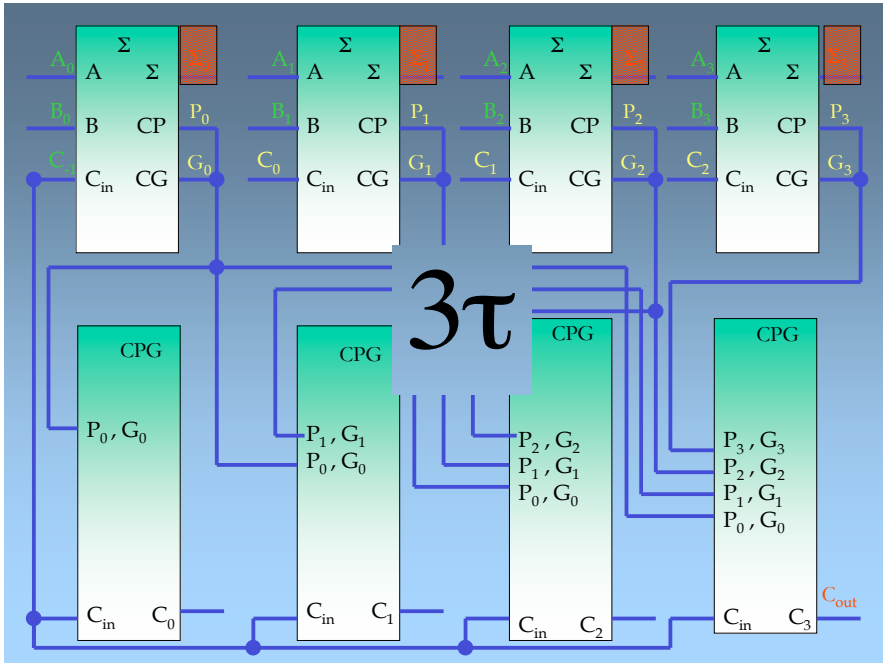


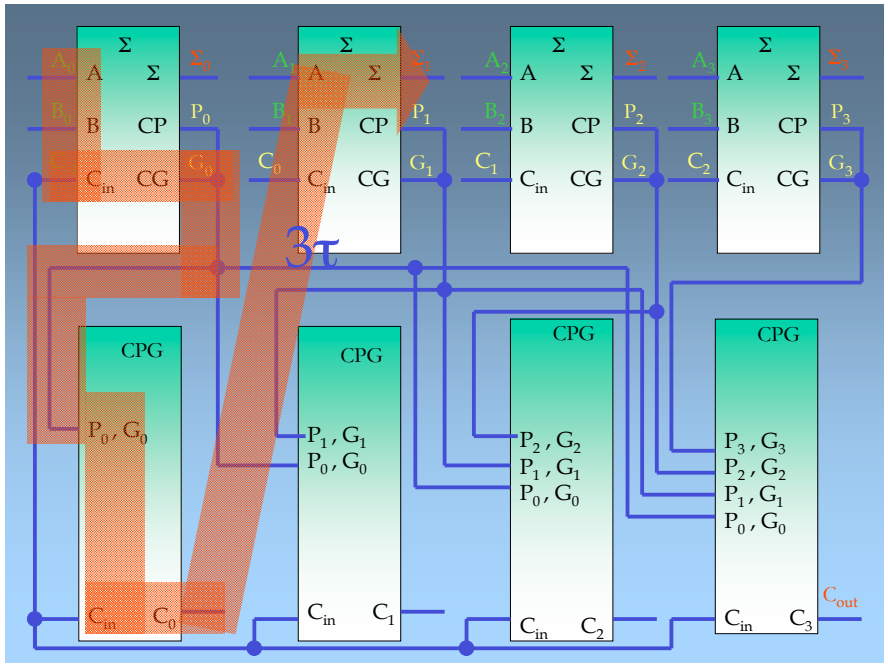



Σ
A
B
CP
Cin
CG
τ
CPG
P0 , G0
P1 , G1
P0 , G0
P2 , G2
P1 , G1
P0 , G0
P3 , G3
P2 , G2
P1 , G1
P0 , G0
Cout


τ
Σ
A
B
CP
Cin
CG
CPG
P0 , G0
P1 , G1
P0 , G0
P2 , G2
P1 , G1
P0 , G0
P3 , G3
P2 , G2
P1 , G1
P0 , G0
Cout


2τ
Σ
A
B
CP
Cin
CG
CPG
P0 , G0
P1 , G1
P0 , G0
P2 , G2
P1 , G1
P0 , G0
P3 , G3
P2 , G2
P1 , G1
P0 , G0
Cout


3τ
Σ
A
B
CP
Cin
CG
CPG
P0 , G0
P1 , G1
P0 , G0
P2 , G2
P1 , G1
P0 , G0
P3 , G3
P2 , G2
P1 , G1
P0 , G0
Cout



Sumadores

- Sumador de propagación del acarreo
  - Más pequeños
  - Rizo del acarreo
  - Tiempo de propagación Nτ
- Sumador de acarreo de grupo hacia adelante
  - Salidas sincronizadas
  - Tiempo de propagación fijo 3τ
  - Ocupan más área (en proporción a N)

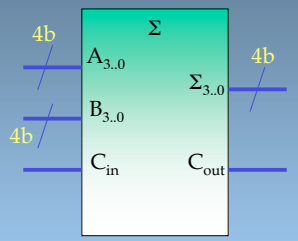
Sumadores

- Sumador de propagación del acarreo
  - Más pequeños
  - Rizo del acarreo
  - Tiempo de propagación Nτ
- Sumador de acarreo de grupo hacia adelante
  - Salidas sincronizadas
  - Tiempo de propagación fijo 3τ
  - Ocupan más área (en proporción a N)

```
  0111
+    1
------
0110 (τ)
0100 (2τ)
0000 (3τ)
1000 (4τ)
```

```
  0111
+    1
------
1000 (3τ)
```

Sumador MSI de 4 bits (Ej. 74x83A ó 74x283)



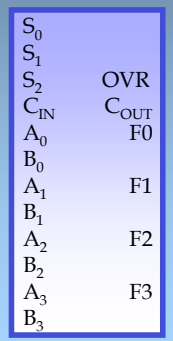
Ejercicio: Implementar un sumador de 16 bits a partir de sumadores de 4 bits

Unidades lógico-aritméticas MSI

ALU de 4bits 74x382

S_2	S_1	S_0	Función
0	0	0	F=0000
0	0	1	F=B menos A menos 1 más C_{in}
0	1	0	F=A menos B menos 1 más C_{in}
0	1	1	F=A más B más C_{in}
1	0	0	F=A⊕B
1	0	1	F=A+B
1	1	0	F=A·B
1	1	1	F=1111

OVR=1 Para desbordamiento con números con signo

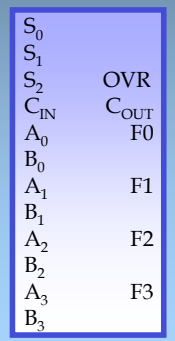


Unidades lógico-aritméticas MSI

ALU de 4bits 74x382

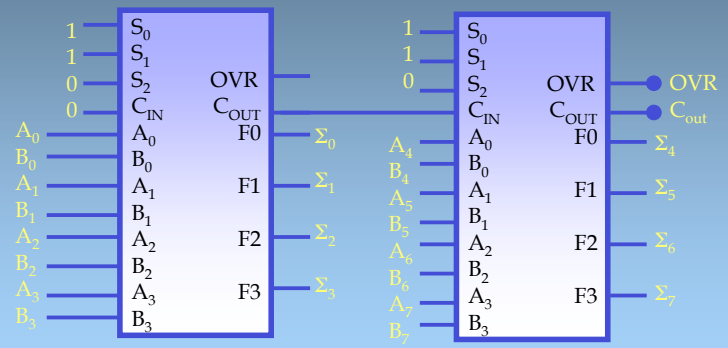
S_2	S_1	S_0	Función
0	0	0	F=0000
0	0	1	F=B menos A menos 1 más C_{in}
0	1	0	F=A menos B menos 1 más C_{in}
0	1	1	F=A más B más C_{in}
1	0	0	F=A⊕B
1	0	1	F=A+B
1	1	0	F=A·B
1	1	1	F=1111

OVR=1 Para desbordamiento con números con signo

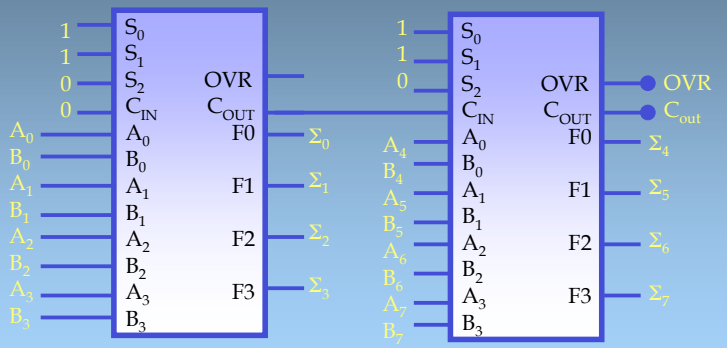


Implementar un sumador de 8 bits

Sumador de 8 bits



Sumador de 8 bits



¿Qué cambios introducirías para hacer un restador?

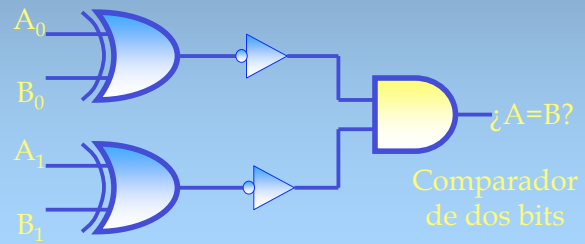
Comparadores

Comparadores

Comparador básico
1 si son distintos
0 si son iguales

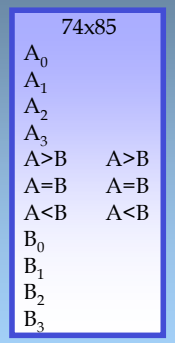
Comparadores

Comparador básico
1 si son distintos
0 si son iguales



Comparador
de dos bits

Comparador de magnitud MSI



Comparador de magnitud MSI

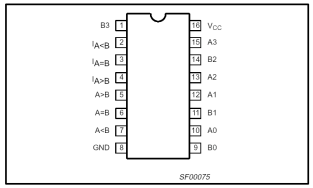
74x85

A_0
A_1
A_2
A_3
A>B A>B
A=B A=B
A<B A<B
B_0
B_1
B_2
B_3

TODA LA INFORMACIÓN EN EL DATASHEETDEL FABRICANTE

Comparador 74x85

PIN CONFIGURATION

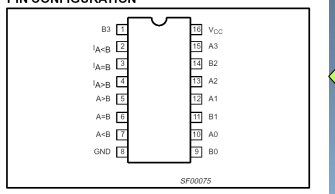


DESCRIPTION

The 74F85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A0–A3) and (B0–B3) where A3 and B3 are the most significant bits. The operation of the 74F85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme. The expansion inputs $I_{A>B}$, and $I_{A=B}$ and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A>B, A=B and A<B outputs of the lease significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation, the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = Low, $I_{A=B}$ = High, and $I_{A<B}$ = Low.

Comparador 74x85

PIN CONFIGURATION



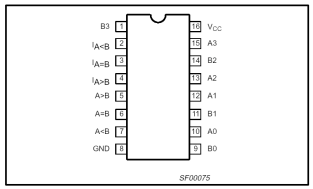
CONFIGURACIÓN DE PINES DEL INTEGRADO: RELACIÓN CON ENTRADAS Y SALIDAS

DESCRIPTION

The 74F85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A0–A3) and (B0–B3) where A3 and B3 are the most significant bits. The operation of the 74F85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme. The expansion inputs $I_{A>B}$, and $I_{A=B}$ and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A>B, A=B and A<B outputs of the lease significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation, the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = Low, $I_{A=B}$ = High, and $I_{A<B}$ = Low.

Comparador 74x85

PIN CONFIGURATION



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DESCRIPTION

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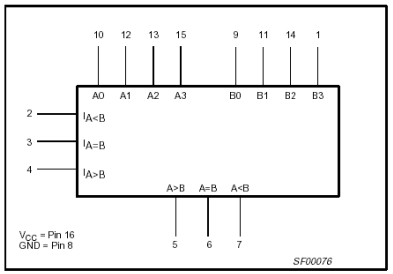
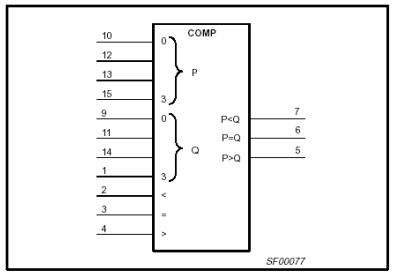
DESCRIPCIÓN DE FUNCIONAMIENTO: TEXTOS EN INGLÉS

Comparador 74x85

LOGIC SYMBOL



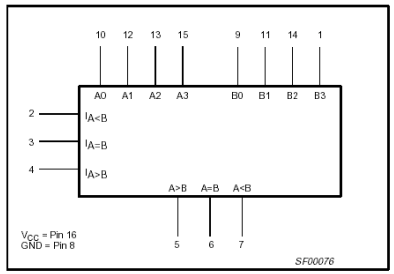
IEC/IEEE SYMBOL



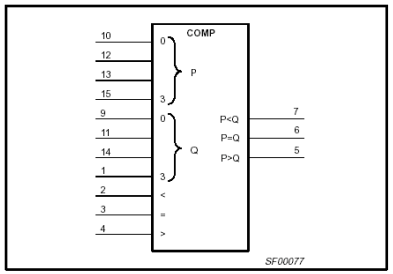
Comparador 74x85

SÍMBOLO ESQUEMÁTICO: CLÁSICO Y ESTÁNDAR IEEE

LOGIC SYMBOL

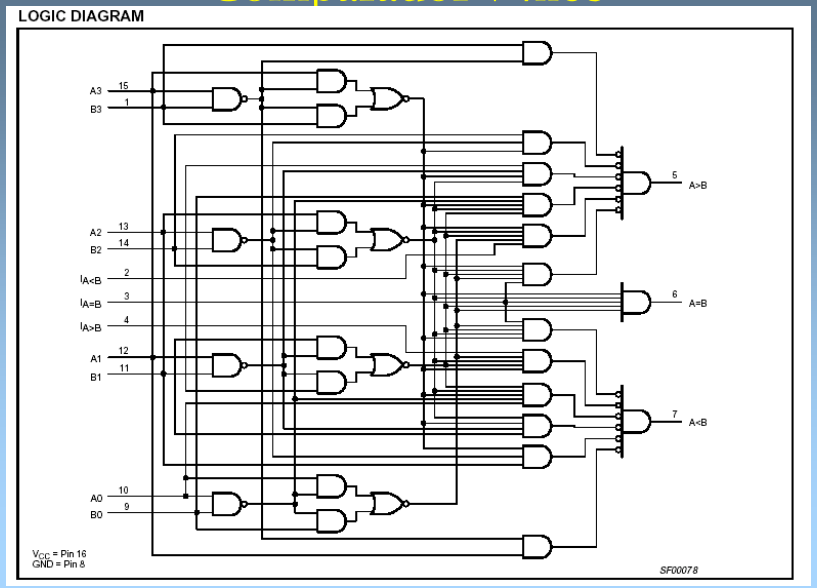


IEC/IEEE SYMBOL



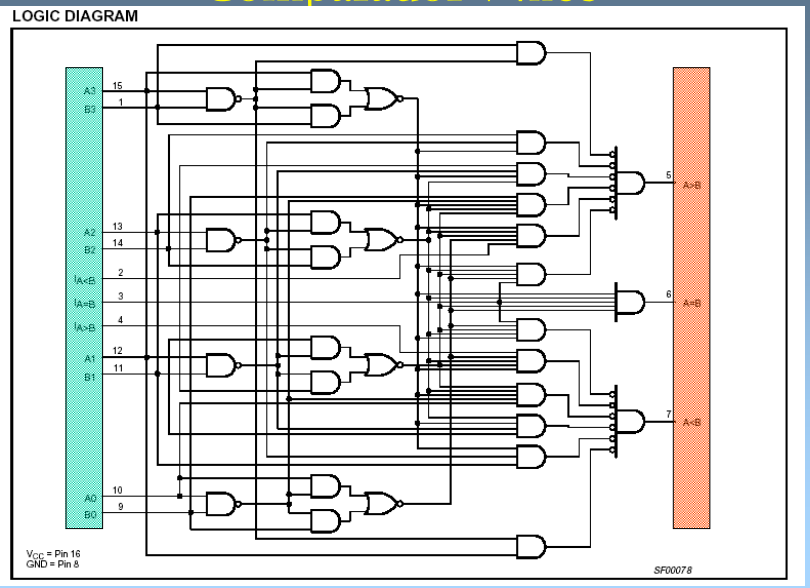
Comparador 74x85

LOGIC DIAGRAM



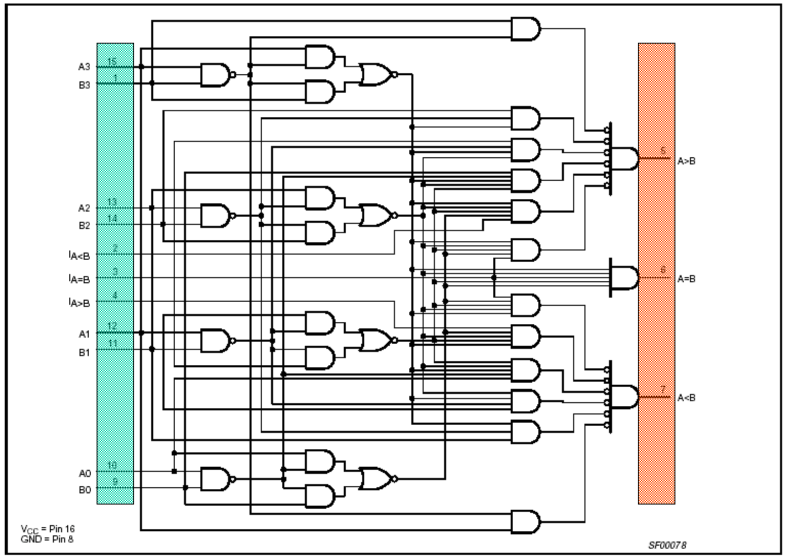
Comparador 74x85

LOGIC DIAGRAM



Comparador 74x85

LOGIC DIAGRAM



Comparador 74x85

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F85	7.0ns	40mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F85N	SOT38-4
16-pin plastic SO	N74F85D	SOT162-1

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16-pin plastic DIP	N74F85N	SOT38-4
16-pin plastic SO	N74F85D	SOT162-1

Comparador 74x85

FUNCTION TABLE

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A3,B3	A2,B2	A1,B1	A0,B0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

Comparador 74x85

FUNCTION TABLE

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A3,B3	A2,B2	A1,B1	A0,B0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

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Comparador 74x85

FUNCTION TABLE

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A3,B3	A2,B2	A1,B1	A0,B0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

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Comparador 74x85

FUNCTION TABLE

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A3,B3	A2,B2	A1,B1	A0,B0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

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Comparador 74x85

FUNCTION TABLE

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A3,B3	A2,B2	A1,B1	A0,B0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

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Comparador 74x85

FUNCTION TABLE

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A3,B3	A2,B2	A1,B1	A0,B0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

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Comparador 74x85

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COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A3,B3	A2,B2	A1,B1	A0,B0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

APPLICATION

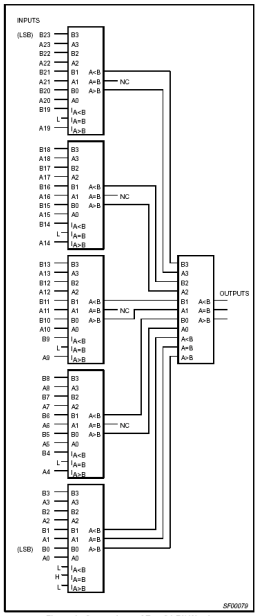
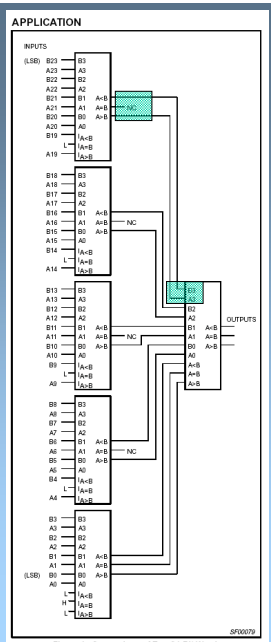


Figure 1. Comparison of Two 24-Bit Words

Configuración en paralelo para comparar dos números de 24 bits

APPLICATION



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APPLICATION

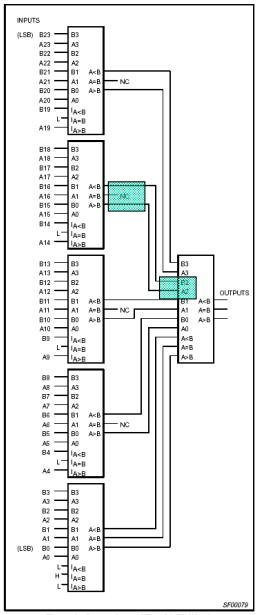

Figure 1. Comparison of Two 24-Bit Words

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APPLICATION

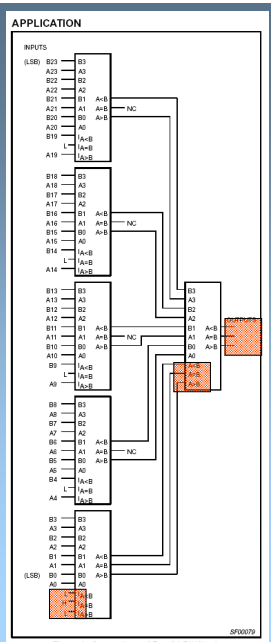
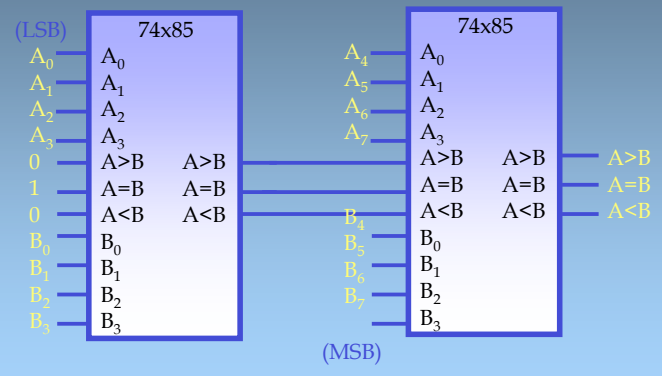


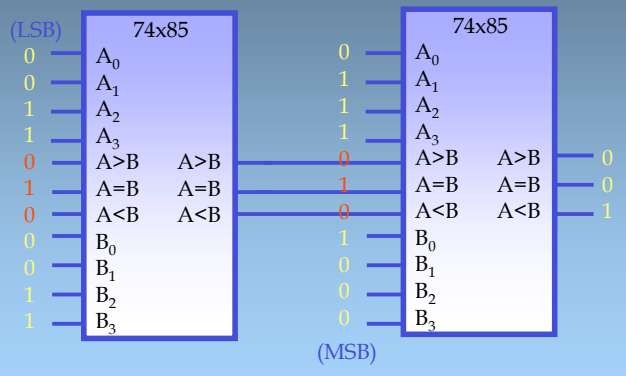
Figure 1. Comparison of Two 24-Bit Words

Configuración en paralelo para comparar dos números de 24 bits

Comparación en serie



Comparación en serie



Comparación en serie