Dispositivos de lógica programable

SISTEMAS ELECTRÓNICOS DIGITALES

2º Curso Ingeniería Técnica Industrial

Especialidad en Electrónica Industrial

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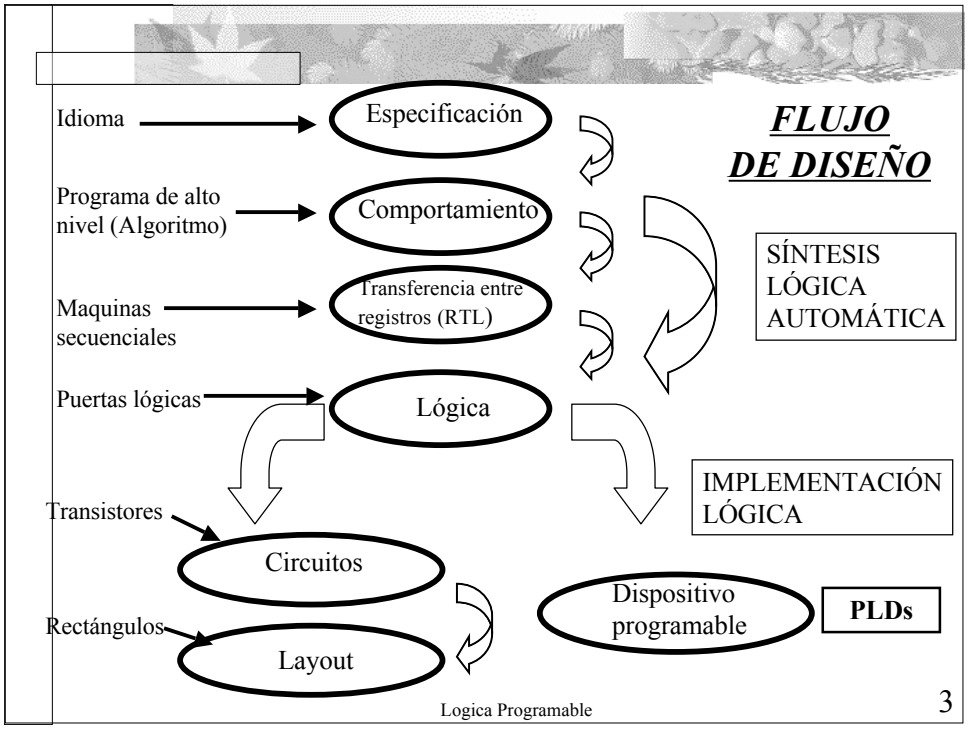


Conceptos generales

- Cada circuito integrado contiene un determinado número de elementos lógicos
- Para cada tipo de aplicación el esquema de interconexiones es fija
- Posibles implementaciones de una aplicación
  - En un circuito específico (ASIC)
  - En un circuito de propósito general (programable)

Logica Programable 4

Fundamento

- Cualquier función lógica puede expresarse como suma de productos

  $F=m_1+m_2+m_3+\ldots=\bar{x}\bar{y}z+z\bar{y}z+\bar{x}yz$

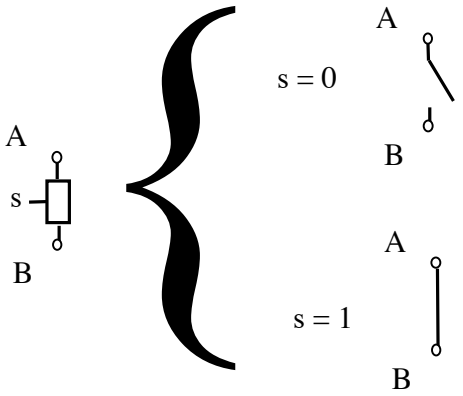
- La función se realiza en dos niveles

  1er nivel ⟹ Producto

  2º nivel ⟹ Suma

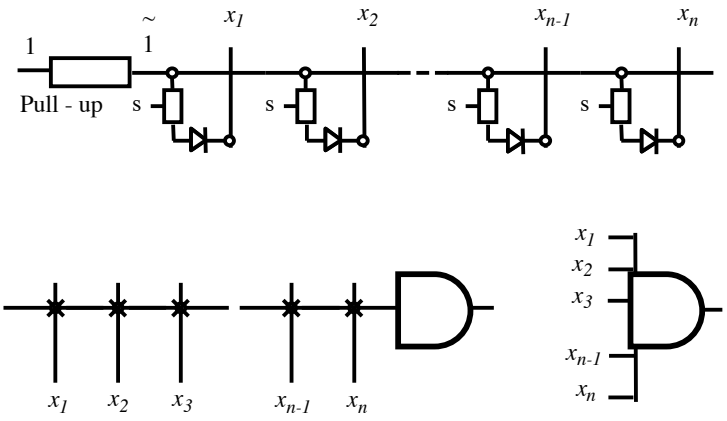
Esquema de conexiones

- Conexión entre líneas mediante un dispositivo programable



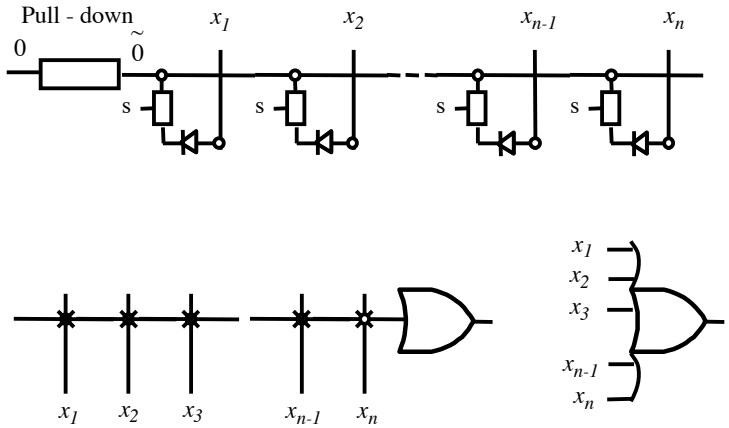
Este elemento conector puede ser un fusible (si la programación de cada interconexión es permanente) o un transistor MOS de doble puerta si queremos que además de programable sea reconfigurable

Modelo de estructura AND



Logica Programable 7

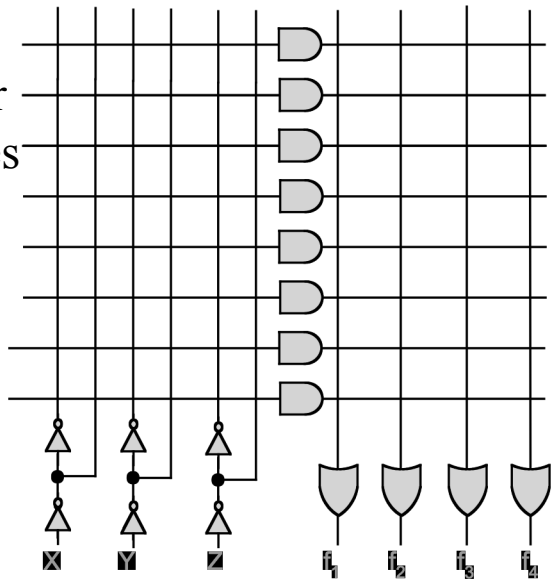
Modelo de estructura OR



Logica Programable 8

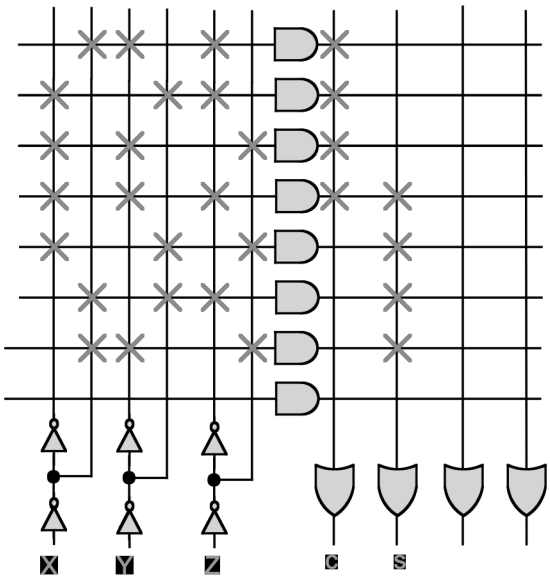
Matriz programamable AND-OR

Permite realizar cuatro funciones logicas de n entradas.



Ejemplo de programación

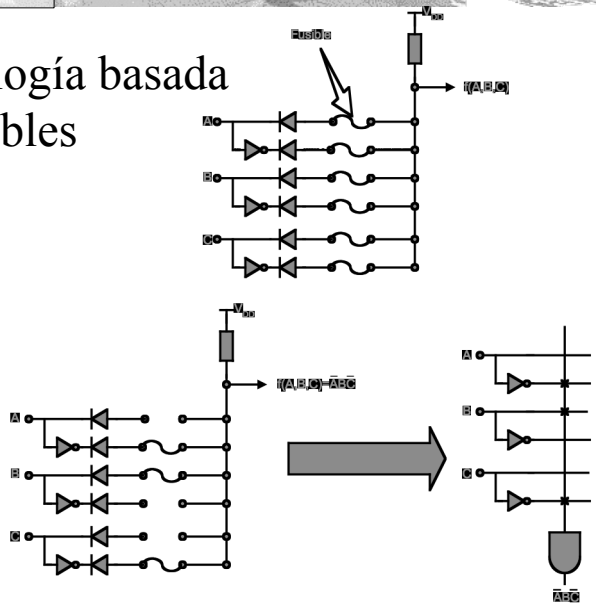
Ejemplo sencillo:
Full adder
$s=xyz+x\bar{y}\bar{z}$
$+\bar{x}\bar{y}z+\bar{x}y\bar{z}$
$c=xyz+\bar{x}yz$
$+x\bar{y}z+xy\bar{z}$



Dispositivos programables

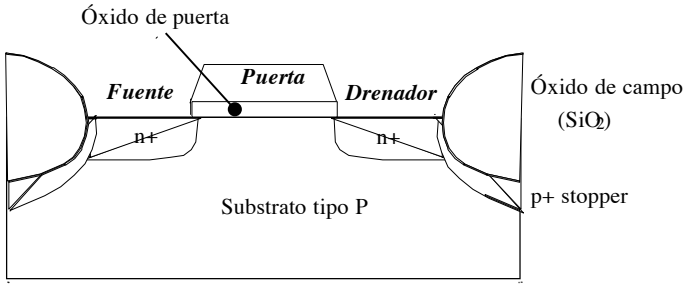
- Tecnología basada en fusibles
  - Programable una sola vez
  - No-Volátil
- Tecnología basada en SRAM
  - Reconfigurable
  - Volátil
- Tecnología EPROM y EEPROM
  - Reconfigurable
  - No-Volátil

Tecnología basada en fusibles



Tecnología EPROM y EEPROM

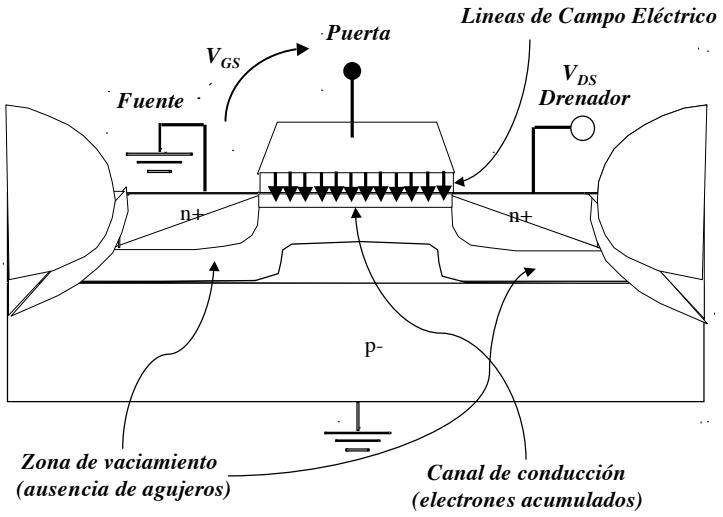
Transistor MOS



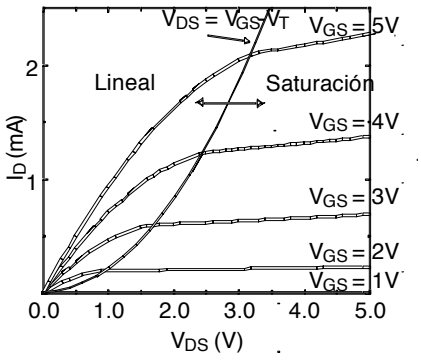
Transistor n-MOS

Tecnología CMOS

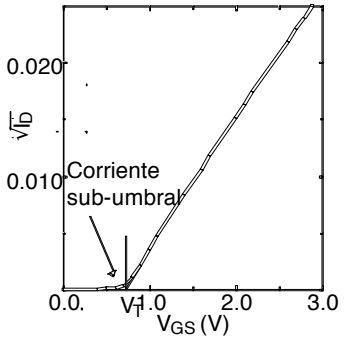
Concepto de Tensión umbral (V_{TH})



Curvas características del transistor n-MOS



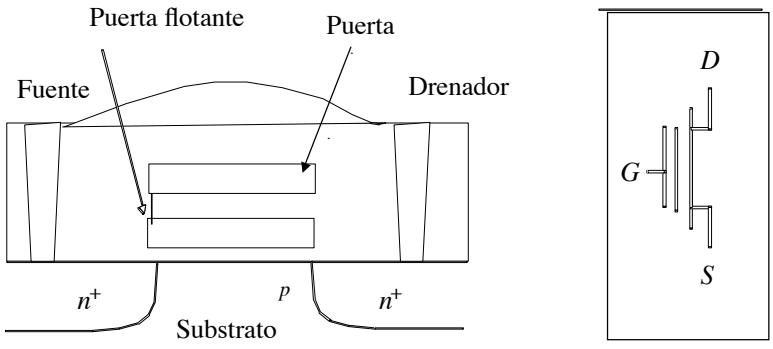
(a) I_D en función de V_{DS}



(b) $\sqrt{I_D}$ en función de V_{GS}
(para V_{DS} = 5V)

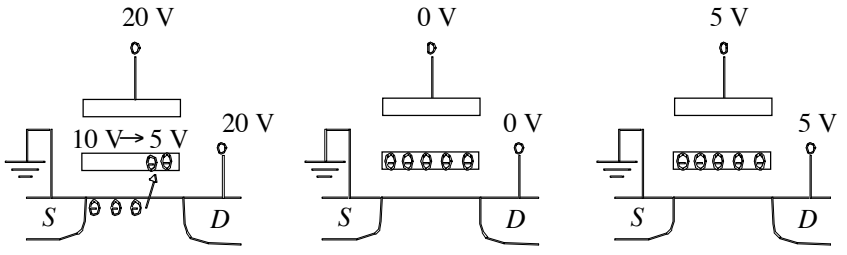
Transistor n-MOS W = 100μm, L = 20μm

Transistor MOS de doble puerta



Símbolo

Programación del transistor de doble puerta

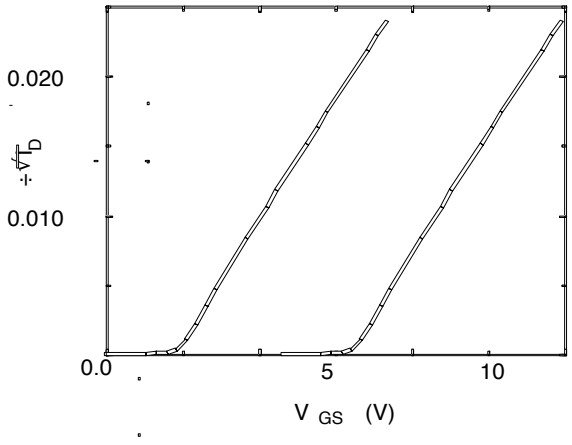


Programación por avalancha

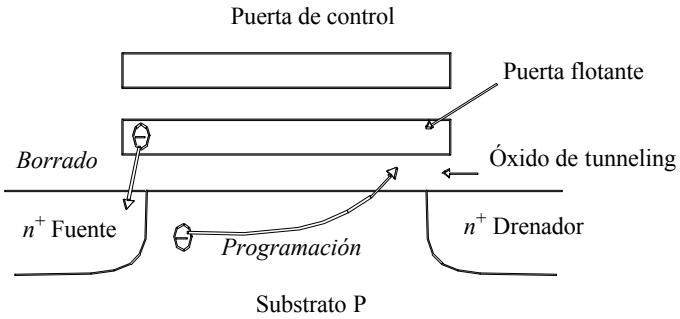
Los electrones quedan atrapados en la puerta flotante

El valor efectivo de la tensión umbral aumenta debido al apantallamiento de los electrones atrapados en la puerta flotante

Desplazamiento de V_{TH}



Flash EEPROM

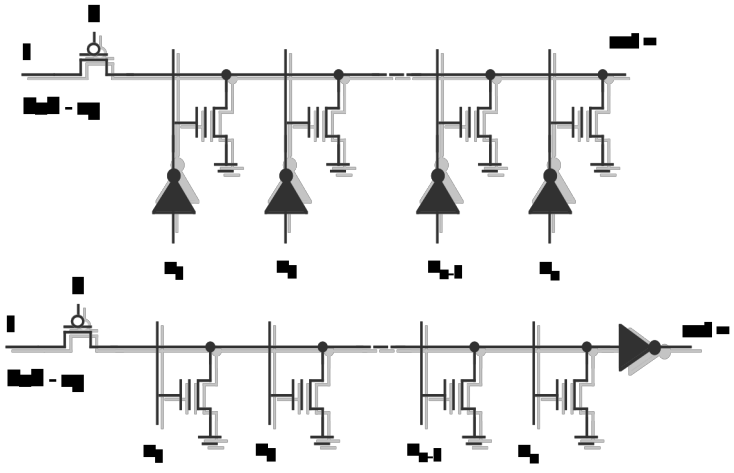


Cross-sections of NVM cells

Flash **EPROM**

Courtesy Intel

Puertas distribuidas (esquema físico)



Tipos de dispositivos programables

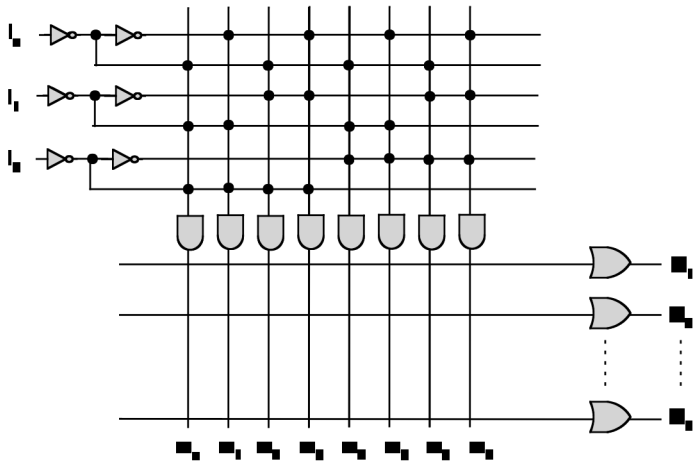
- PROM: Matriz OR programable y AND no programable
- FPLA: Matriz AND y OR programables
- PAL: Matriz AND programable y OR no programable

PROM

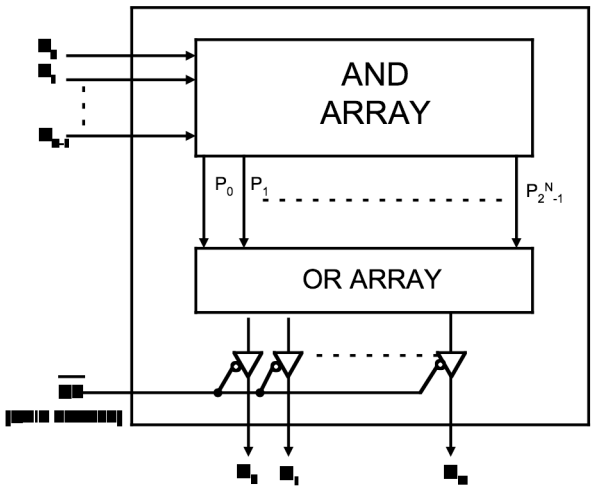
Matriz OR programable y AND no programable

- Más rápidas si se comparan con otros tipos de lógica
- Ideales si hemos de implementar funciones que usan todos los mintérminos
  Codificadores, Look-up tables
- Para n entradas tenemos 2n puertas AND
  Bastante extensas para n grande

PROMs



Esquema básico de una PROM



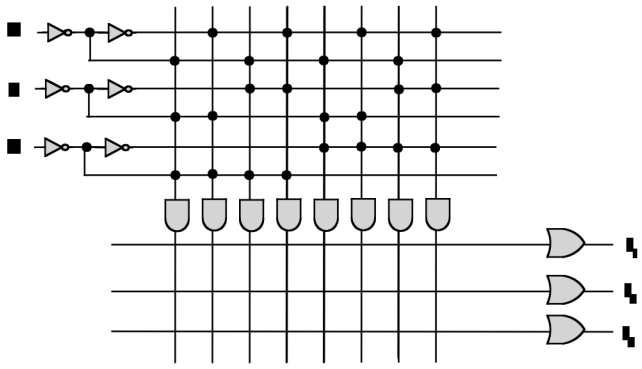
Problema 1:

- Implementar en las siguientes funciones:

$f_1=AB+\overline{B}C$

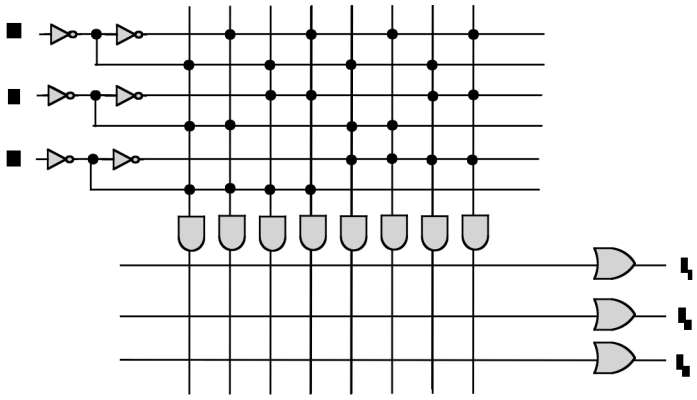
$f_2=(A+\overline{B}+C)(\overline{A}+B)$

$f_3=A+BC$



Problema 2:

- Implementar un conversor de binario a código gray



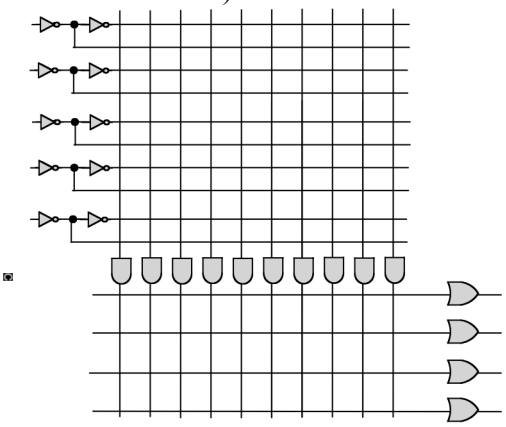
FPLA

Matriz OR y AND programables

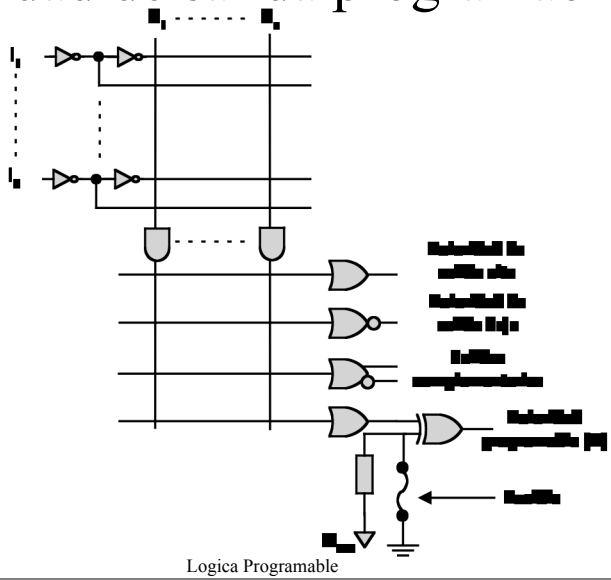
- Más pequeñas y flexibles que las PROM
- Cualquier término producto puede ser programado (no sólo mintérminos)
- Más lentas al tener una etapa más para ser programada

Problema: Voto mayoritario

- Programa la PLA de forma que proporcione el sentido del voto mayoritario de un total de cinco electores (cada voto consiste en un sí o un no).



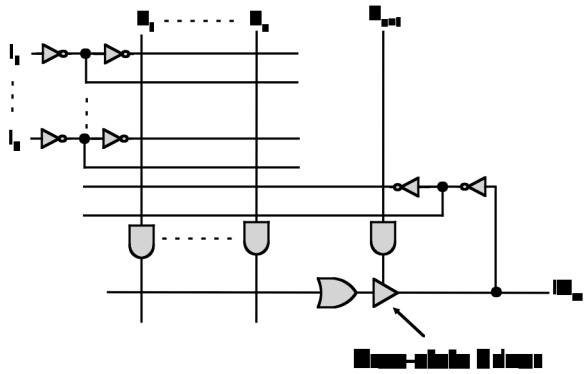
Polaridad de salida programable

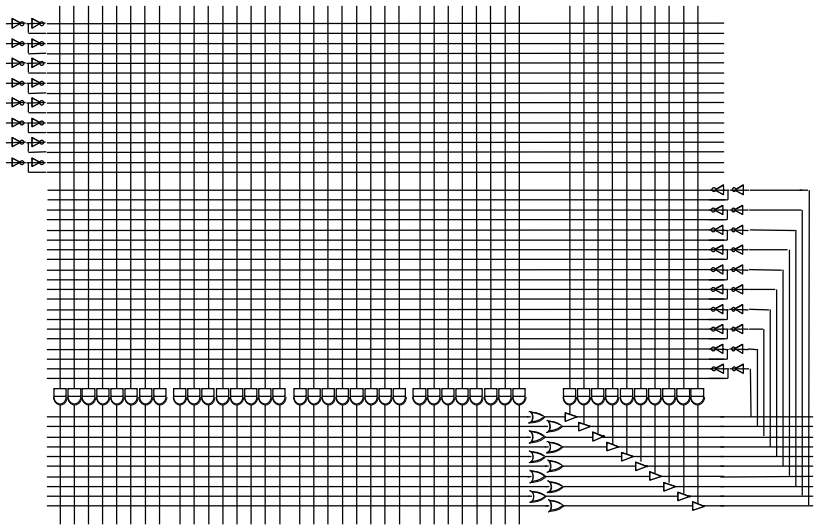


Extensión de la PLAs

- Circuitos basados en la estructura AND-OR modificada de forma que:
  - Permiten terminales bidireccionales
  - Permiten la utilización de variables intermedias

Pines bidireccionales y líneas de realimentación

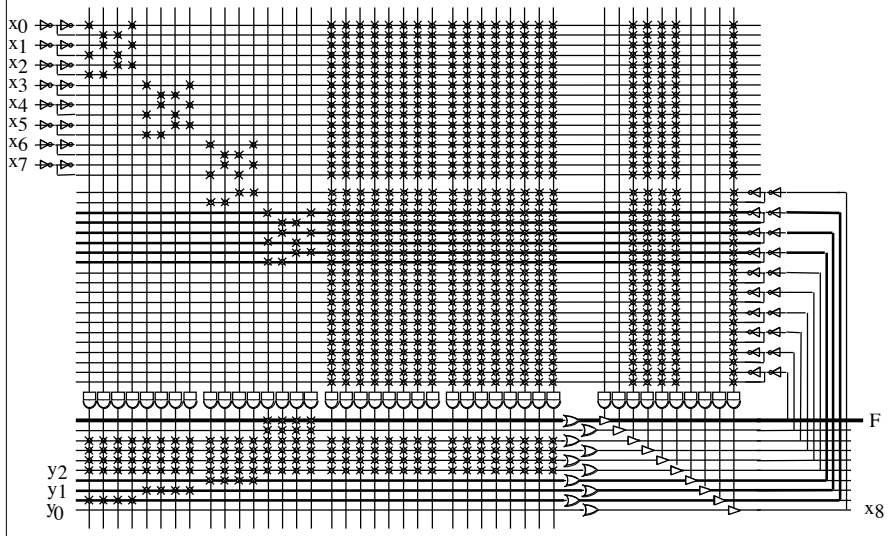




Ejemplo: Función paridad de 9 bits

- $F = x_0 \oplus x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus x_5 \oplus x_6 \oplus x_7 \oplus x_8$
- Implementación a 2 niveles : 256 mintérminos
- Implementación multinivel

$$y_0 = x_0 \oplus x_1 \oplus x_2$$
$$y_1 = x_3 \oplus x_4 \oplus x_5$$
$$y_2 = x_6 \oplus x_7 \oplus x_8$$
$$F = y_0 \oplus y_1 \oplus y_2$$

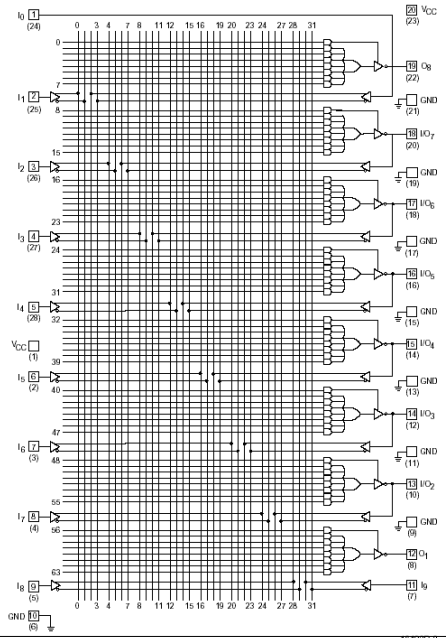


PAL

Matriz AND programable y OR no programable

- Compromiso entre las FPLA y PROMs (más rápidas que las FPLA y no tan grandes como las PROMs)
- Los términos productos comunes a varias funciones tienen que ser implementados por duplicado

PAL comercial: PAL16L8



Problema: Programación de un comparador de 4 bits

- Programar una PAL16L8 de forma que compare dos números de cuatro bits. El sistema ha de producir tres salidas (X,Y,Z), donde X=1 sólo cuando A=B, Y=1 sólo cuando A>B y Z=1 sólo cuando A<B.

Solución:

$X=E_3E_2E_1E_0$

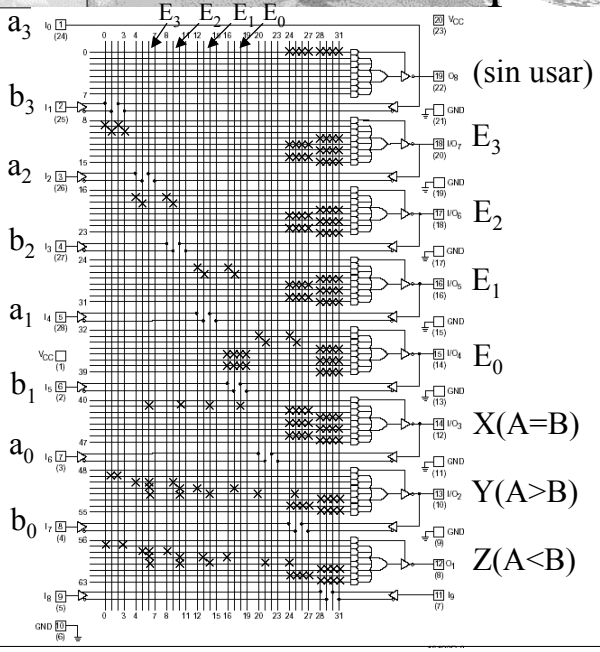
$Y=a_3\overline{b}_3+E_3a_2\overline{b}_2+E_3E_2a_1\overline{b}_1+E_3E_2E_1a_0\overline{b}_0$

$Z=\overline{a}_3b_3+E_3\overline{a}_2b_2+E_3E_2\overline{a}_1b_1+E_3E_2E_1\overline{a}_0b_0$

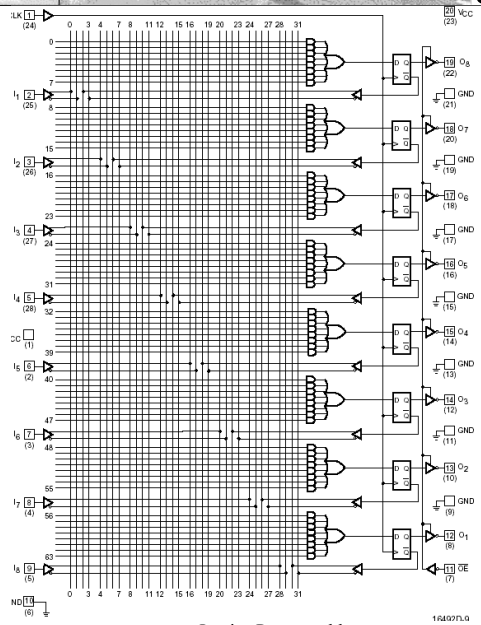
Donde E_i evalua si los bits a_i y b_i son iguales o no.

$E_i=\overline{a}_i\overline{b}_i+a_ib_i$

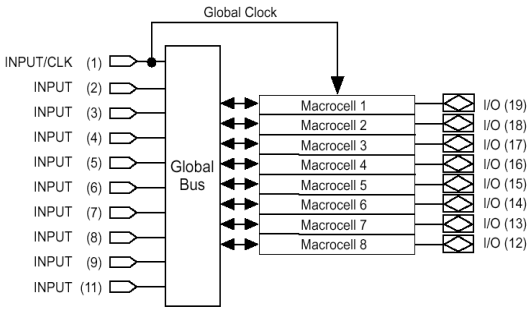
Implementación del comparador

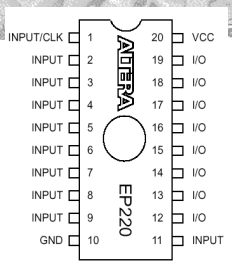


PAL16R8. Salida con resgistros

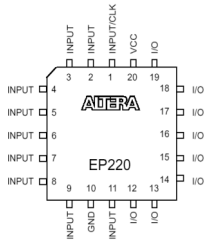


PLDs Complejas





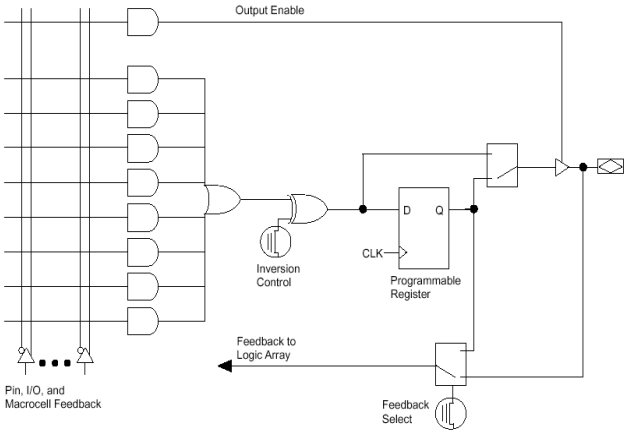
20-Pin DIP

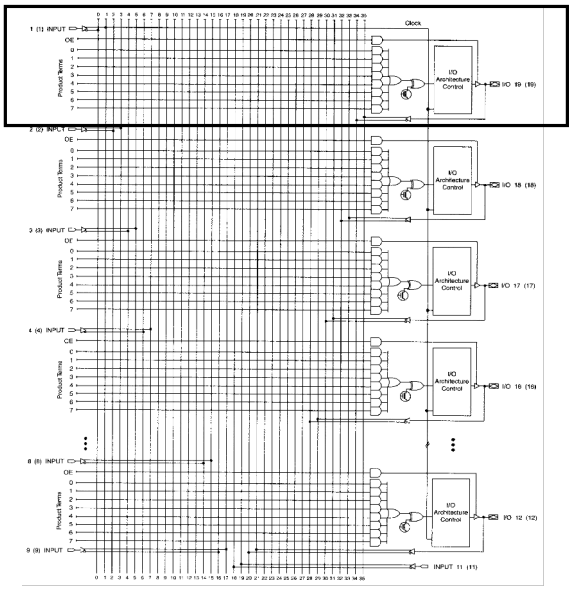


20-Pin J-Lead

Estructura de las macro celdas

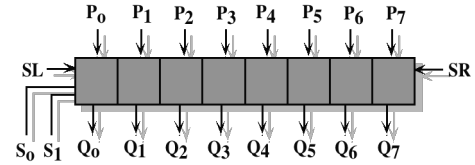
- Introducción de módulos secuenciales en las macro-celdas

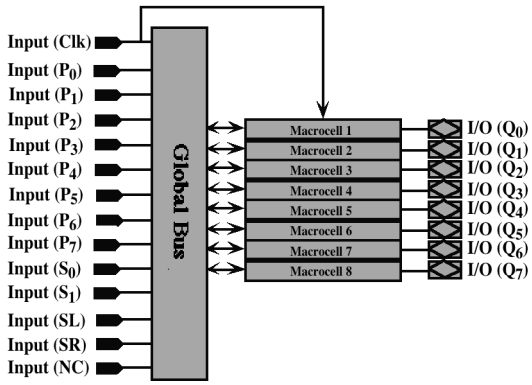




Macrocell

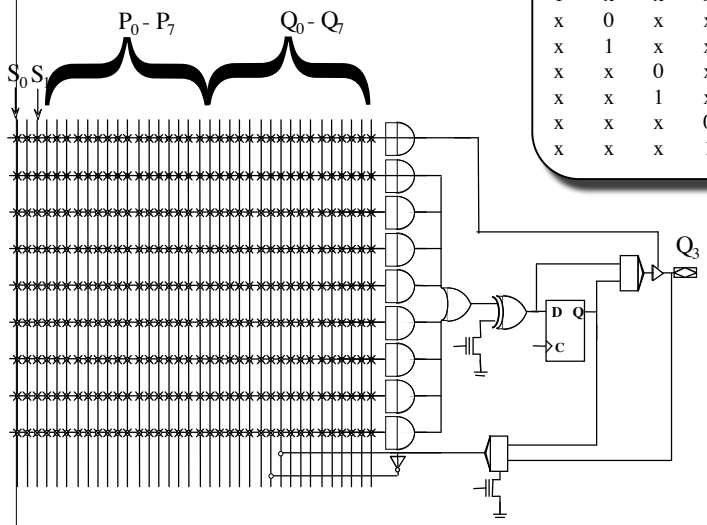
Programación registro universal de 8 bits en EP224



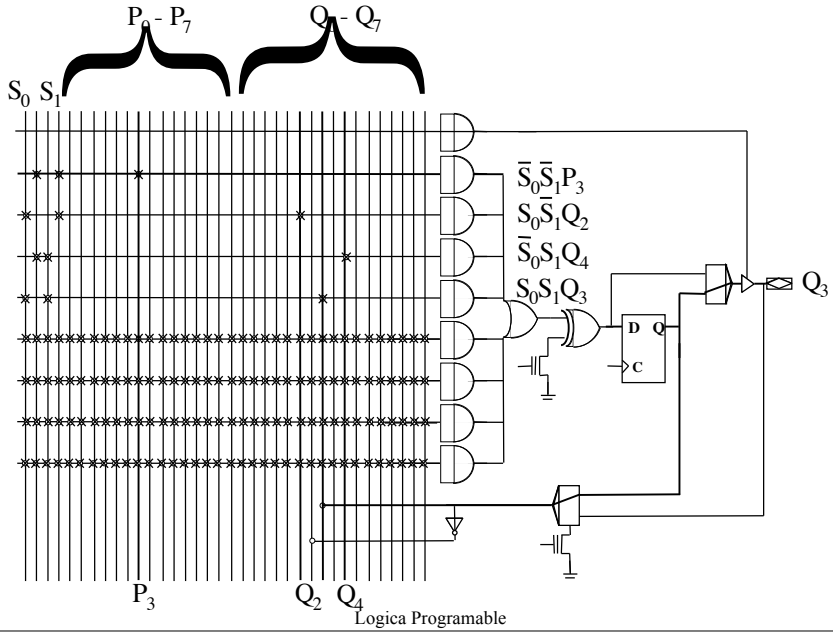


Esquema por macro-celda

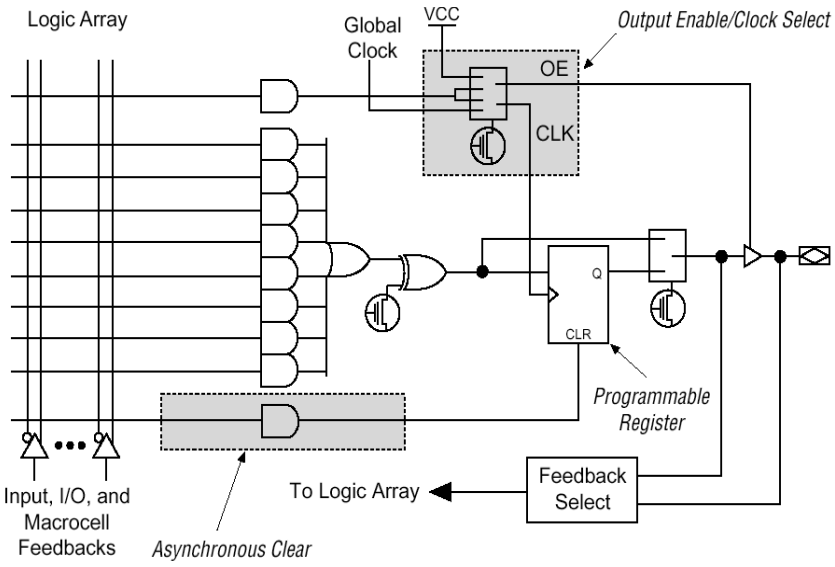
Load P3	SL Q2	SR Q4	Mem Q3	S1	S0	out Q3'
0	x	x	x	0	0	0
1	x	x	x	0	0	1
x	0	x	x	0	1	0
x	1	x	x	0	1	1
x	x	0	x	1	0	0
x	x	1	x	1	0	1
x	x	x	0	1	1	0
x	x	x	1	1	1	1



Programación salida Q3

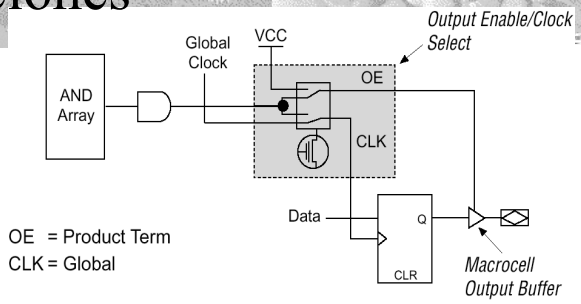


Arquitectura "Classic" de Altera

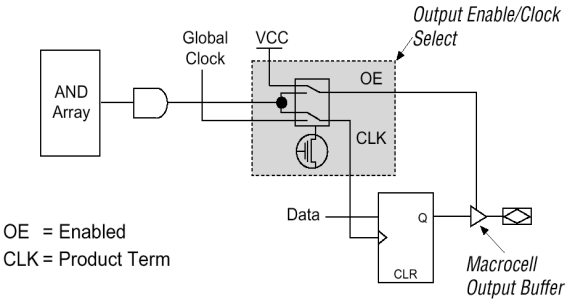


Configuraciones

Modo 0:
Registro controlado por el reloj global.
La salida se controla por la lógica del término producto



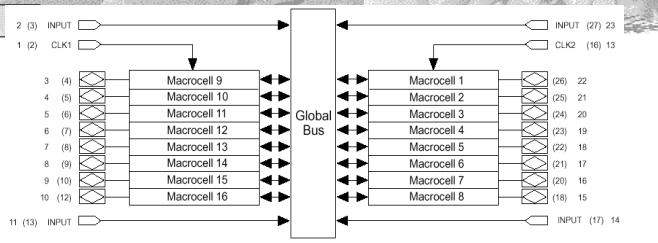
Modo 1:
La salida se encuentra permanentemente habilitada.
El reloj se controla por la lógica del término producto



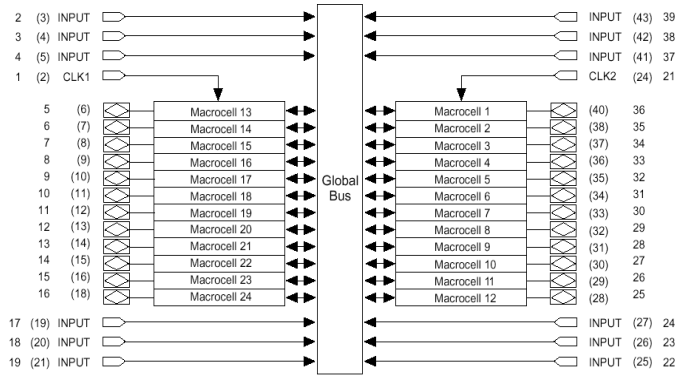
Logica Programable 49

Integrados "Classic" de Altera

EP610 EPLD
300 puertas equiv.
2 Clks indep
16 macro-celdas
tpd = 10ns
freq = 100 MHz

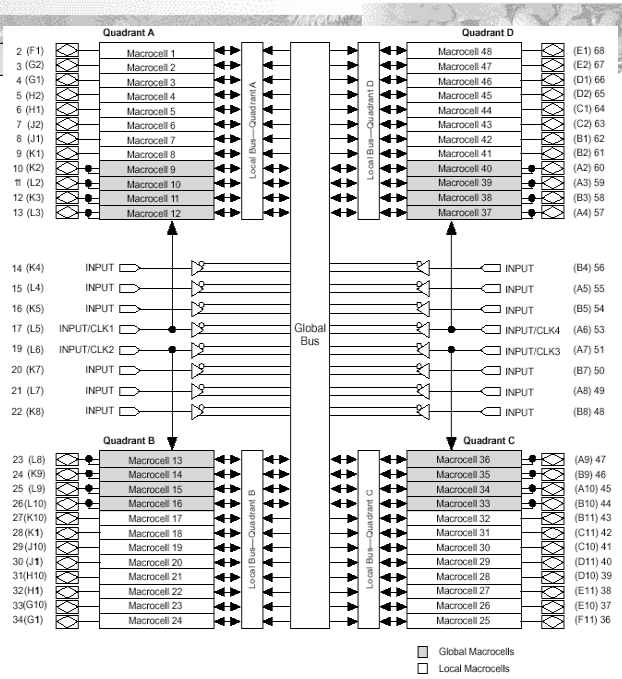


EP910 EPLD
450 puertas equiv.
2 Clks indep
24 macro-celdas
tpd = 12ns
freq = 76.9 MHz



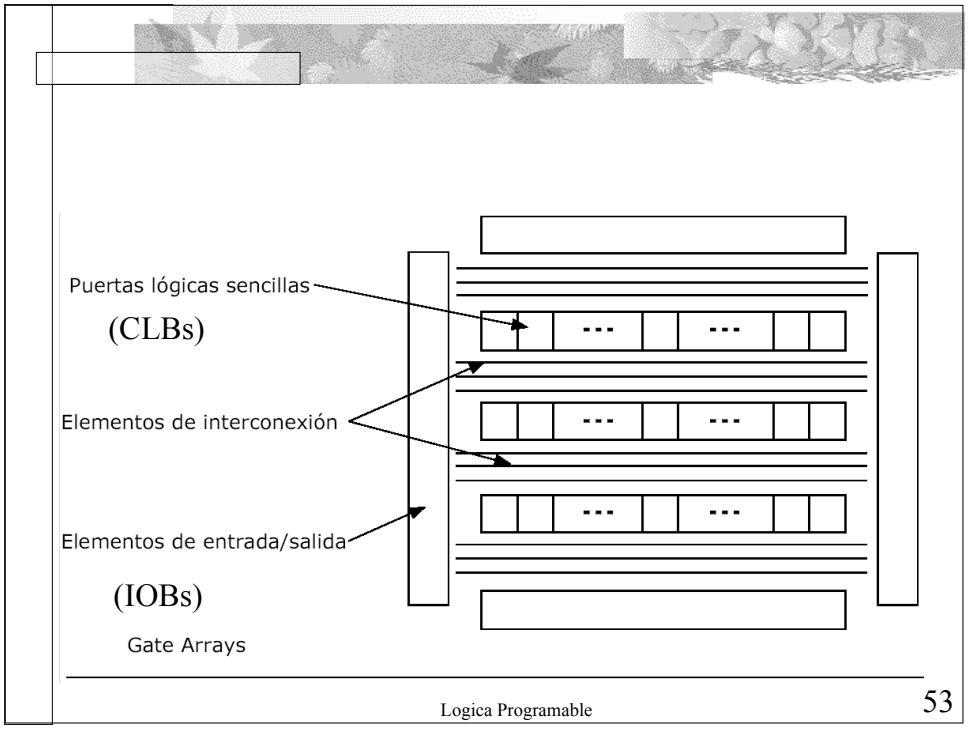
Logica Programable 50

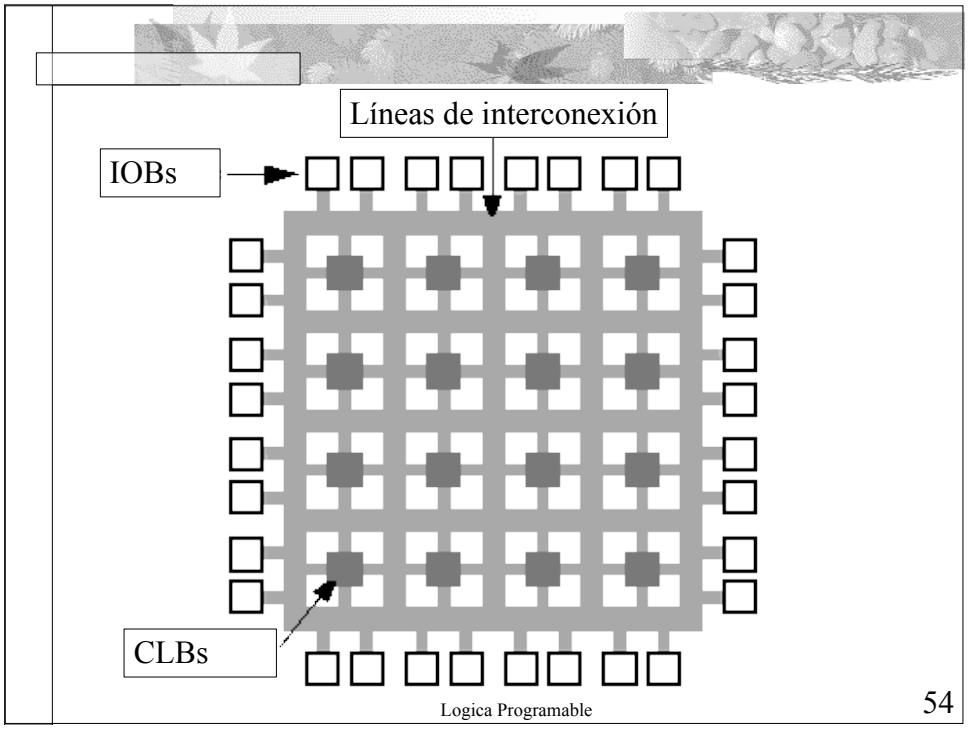
EP1810 EPLD
900 puertas equiv.
4 Clks indep
48 macro-celdas
tpd = 20ns
freq = 50 MHz

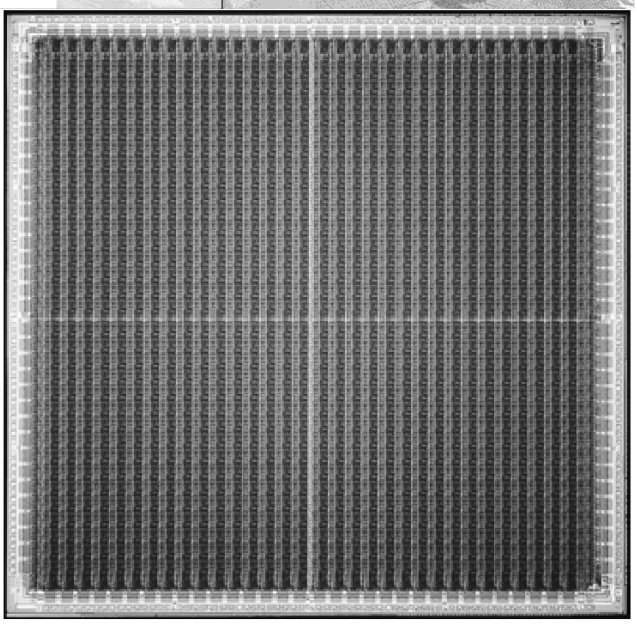


Evolución de las PLAs: Las FPGAs

- Contenido de las FPGAs:
  - Matriz de celdas regularmente dispuestas sobre silicio cuya funcionalidad es progamable (las llamamos CLB)
  - Colección de celdas programables de entrada-salida dispuestas perimetralmente y que deonomnamos IOB
  - Colección de bloques de interconexión que, bajo programación permiten conectar CLBs e IOBs entre sí


Puertas lógicas sencillas
(CLBs)
Elementos de interconexión
Elementos de entrada/salida
(IOBs)
Gate Arrays
Logica Programable
53


Líneas de interconexión
IOBs
CLBs
Logica Programable
54



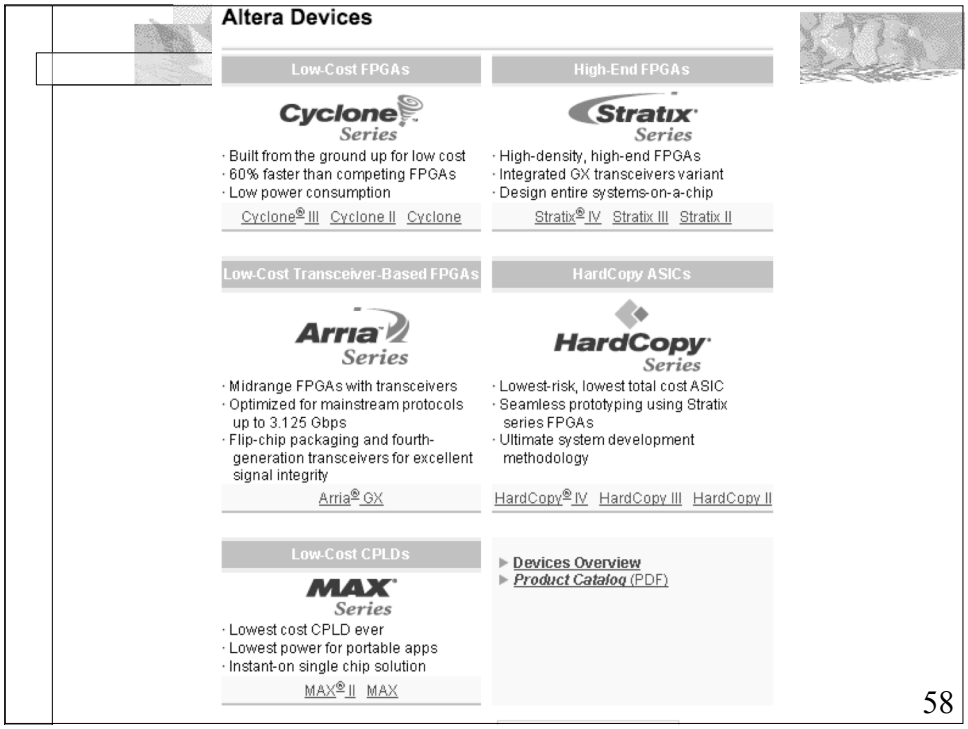
Xilinx XC4025

Tipos de tecnología usada

Tecnología	Volátil	Re-Prog
SRAM	Sí	Sí
PLICE (Fusibles)	No	No
EPROM	No	Sí
EEPROM	No	Sí

FPGAs comerciales

- Altera (MAX, FLEX, ACEX, Cyclone, APEX,….)
- Xilinx (XC2000, XC8100, …)
- Actel (ACT 1-4, 3200DX, 1200XL,…)
- Cross Point (CP20)
- Concurrent Logic (CLi6000)
- Quick Logic (pASIC)
- Intel (iFX780)
- AMD (MACH1,2,3,4,5)
- ATMEL (ATV)
- Pilkingston (Serie TS)
- Zycad Gatefield (Serie GF)

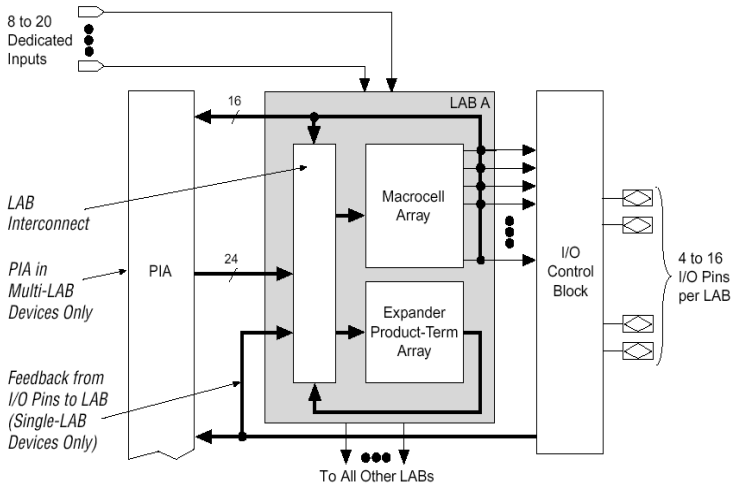


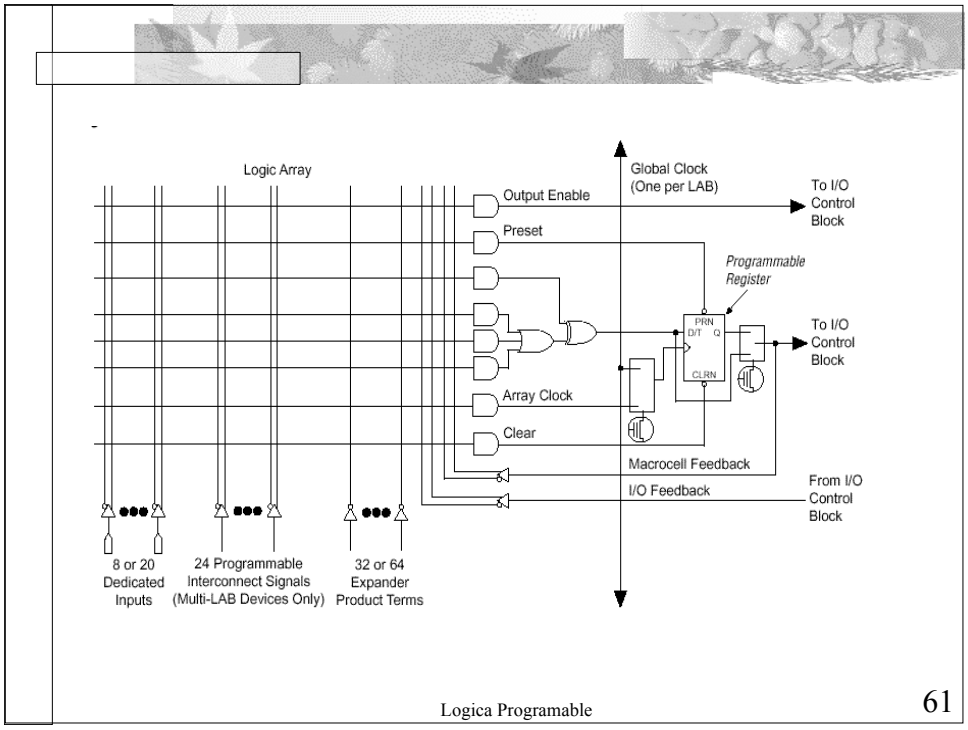
Ejemplo de FPGA comercial, Família MAX5000 (Multiple Array Matrix)de Altera

Table 1. MAX 5000 Device Features

Feature	EPM5032	EPM5064	EPM5128	EPM5130	EPM5192
Usable gates	600	1,250	2,500	2,500	3,750
Macrocells	32	64	128	128	192
Logic array blocks (LABs)	1	4	8	8	12
Expanders	64	128	256	256	384
Routing	Global	PIA	PIA	PIA	PIA
Maximum user I/O pins	24	36	60	84	72
t_{PD} (ns)	15	25	25	25	25
t_{ASU} (ns)	4	4	4	4	4
t_{CO} (ns)	10	14	14	14	14
f_{CNT} (MHz)	76.9	50	50	50	50

Arquitectura del los bloques básicos (LAB)





Componentes de expansión y control I/O

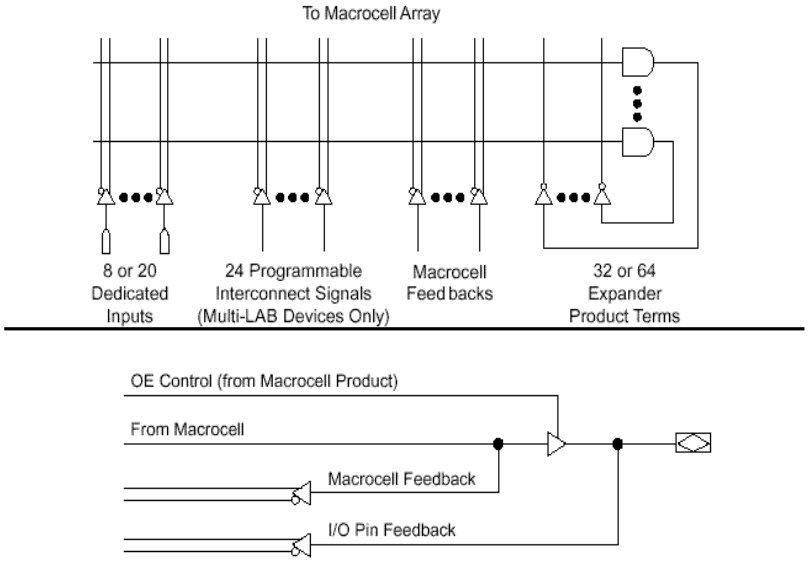


Table 1–1. Cyclone II FPGA Family Features (Part 1 of 2)

Feature	EP2C5 (2)	EP2C8 (2)	EP2C15 (1)	EP2C20 (2)	EP2C35	EP2C50	EP2C70
LEs	4,608	8,256	14,448	18,752	33,216	50,528	68,416
M4K RAM blocks (4 Kbits plus 512 parity bits	26	36	52	52	105	129	250
Total RAM bits	119,808	165,888	239,616	239,616	483,840	594,432	1,152,000
Embedded multipliers (3)	13	18	26	26	35	86	150
PLLs	2	2	4	4	4	4	4

Table 1–1. Cyclone II FPGA Family Features (Part 2 of 2)

Feature	EP2C5 (2)	EP2C8 (2)	EP2C15 (1)	EP2C20 (2)	EP2C35	EP2C50	EP2C70
Maximum user I/O pins	158	182	315	315	475	450	622

Logica Programable 63

Table 1–2. Cyclone II Package Options & Maximum User I/O Pins Notes (1) (2)

Device	144-Pin TQFP (3)	208-Pin PQFP (4)	240-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA	484-Pin Ultra FineLine BGA	672-Pin FineLine BGA	896-Pin FineLine BGA
EP2C5 (6) (8)	89	142	—	158 (5)	—	—	—	—
EP2C8 (6)	85	138	—	182	—	—	—	—
EP2C8A (6), (7)	—	—	—	182	—	—	—	—
EP2C15A (6), (7)	—	—	—	152	315	—	—	—
EP2C20 (6)	—	—	142	152	315	—	—	—
EP2C20A (6), (7)	—	—	—	152	315	—	—	—
EP2C35 (6)	—	—	—	—	322	322	475	—
EP2C50 (6)	—	—	—	—	294	294	450	—
EP2C70 (6)	—	—	—	—	—	—	422	622

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Figure 2–1. Cyclone II EP2C20 Device Block Diagram

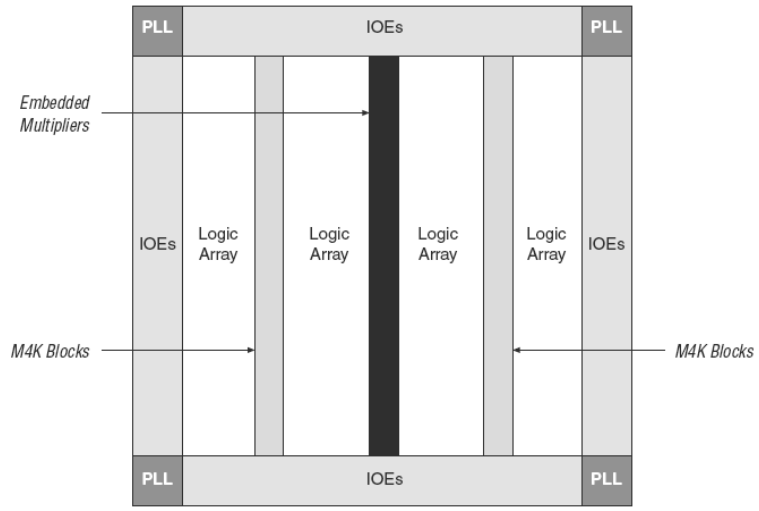


Figure 2–2. Cyclone II LE

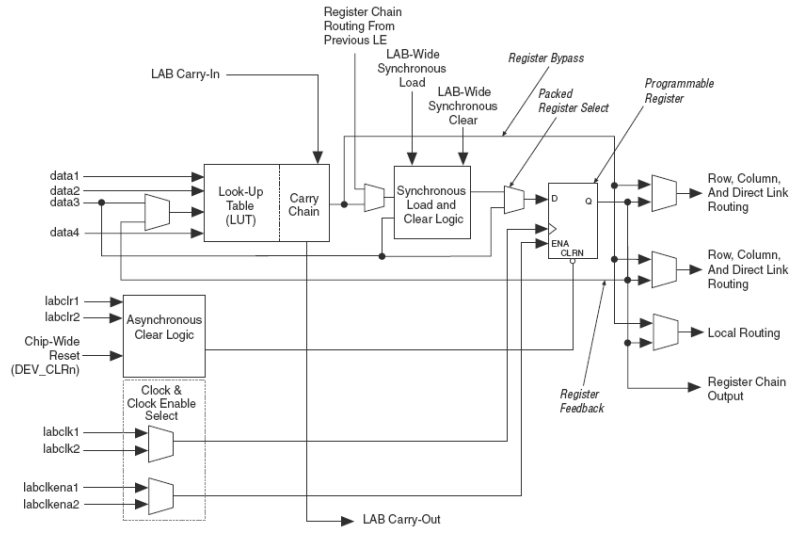
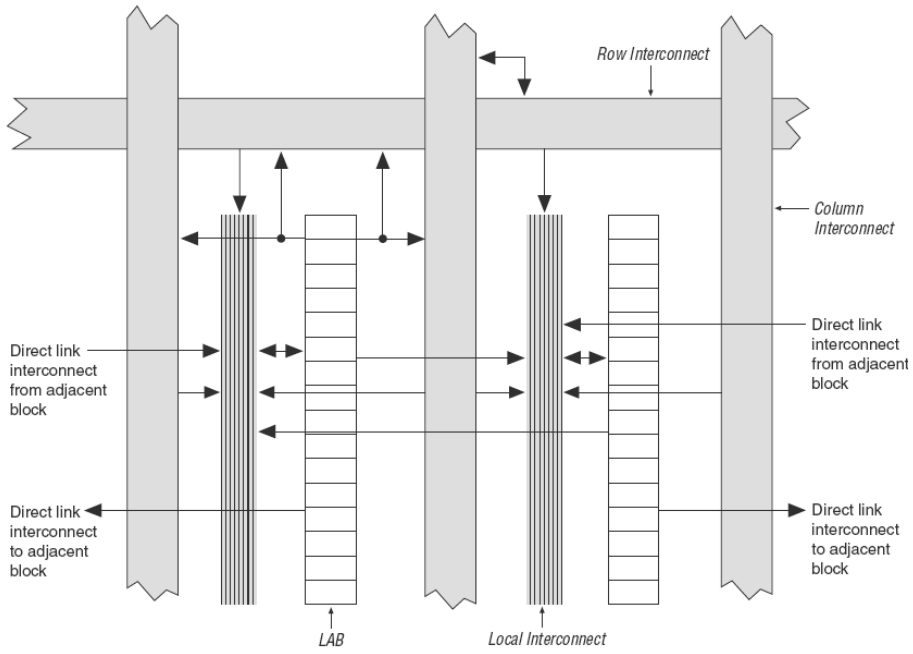


Figure 2–5. Cyclone II LAB Structure



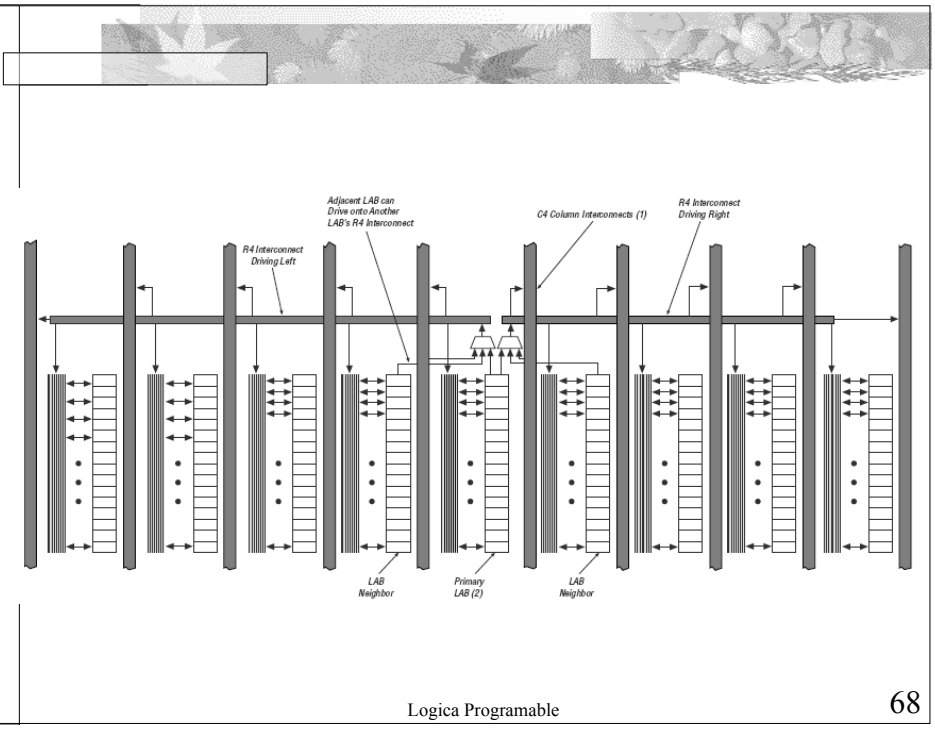


Table 2–4. Cyclone II PLL Features

Feature	Description
Clock multiplication and division	*m* / (*n* × post-scale counter) *m* and post-scale counter values (C0 to C2) range from 1 to 32. *n* ranges from 1 to 4.
Phase shift	Cyclone II PLLs have an advanced clock shift capability that enables programmable phase shifts in increments of at least 45°. The finest resolution of phase shifting is determined by the voltage control oscillator (VCO) period divided by 8 (for example, 1/1000 MHz/8 = down to 125-ps increments).
Programmable duty cycle	The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each PLL post-scale counter (C0-C2).

Figure 2–17. M4K RAM Block LAB Row Interface

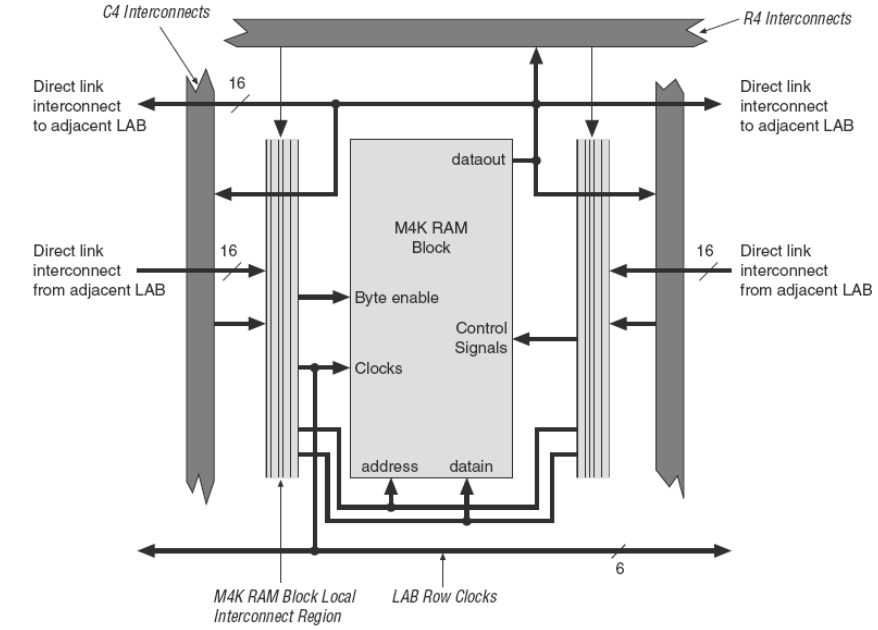
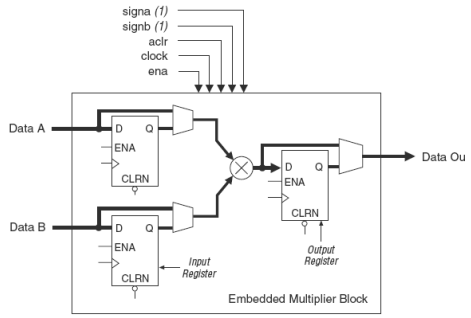
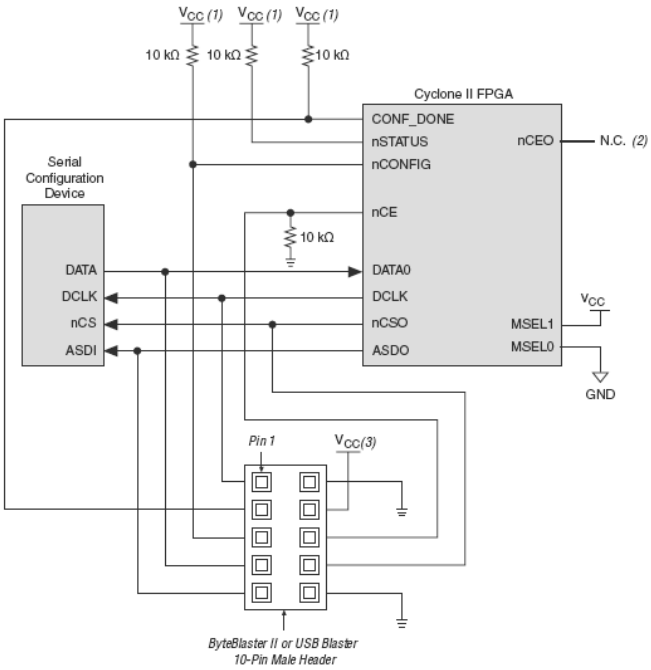


Table 2–10. Number of Embedded Multipliers in Cyclone II Devices *Note (1)*

Device	Embedded Multiplier Columns	Embedded Multipliers	9 × 9 Multipliers	18 × 18 Multipliers
EP2C5	1	13	26	13
EP2C8	1	18	36	18
EP2C15	1	26	52	26
EP2C20	1	26	52	26
EP2C35	1	35	70	35
EP2C50	2	86	172	86
EP2C70	3	150	300	150

Figure 2–18. Multiplier Block Architecture





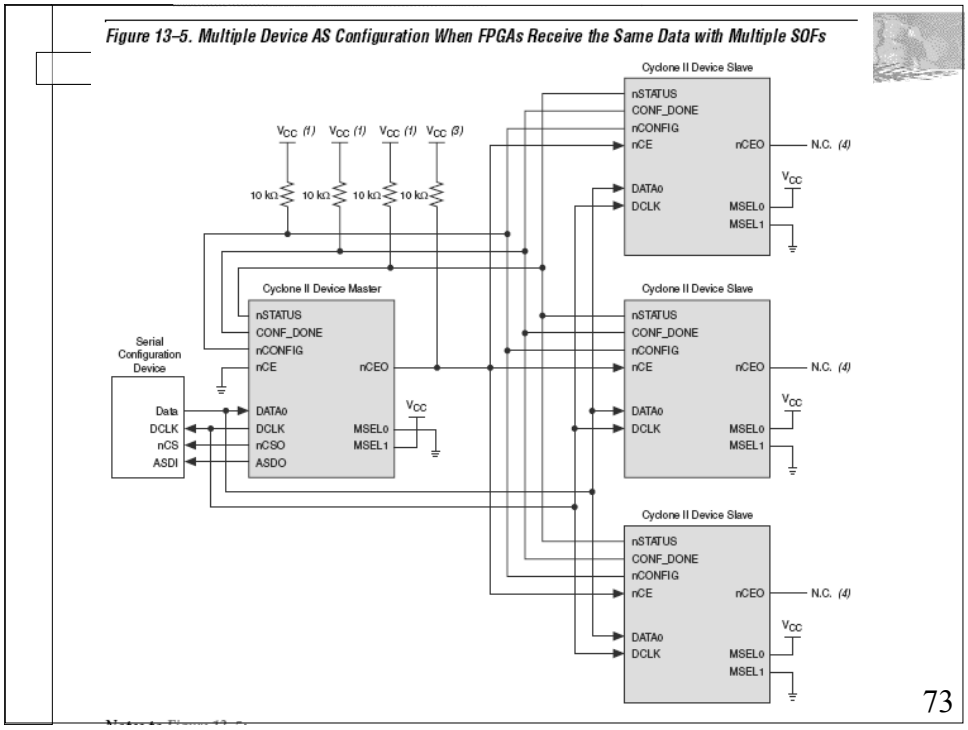


Figure 13–5. Multiple Device AS Configuration When FPGAs Receive the Same Data with Multiple SOFs
Cyclone II Device Slave
nSTATUS
CONF_DONE
nCONFIG
nCE
nCEO
N.C. (4)
DATA0
DCLK
MSEL0
MSEL1
VCC (1)
VCC (1)
VCC (1)
VCC (3)
10 kΩ
10 kΩ
10 kΩ
10 kΩ
VCC
Cyclone II Device Master
Serial Configuration Device
Data
DCLK
nCS
ASDI
nCSO
ASDO
73

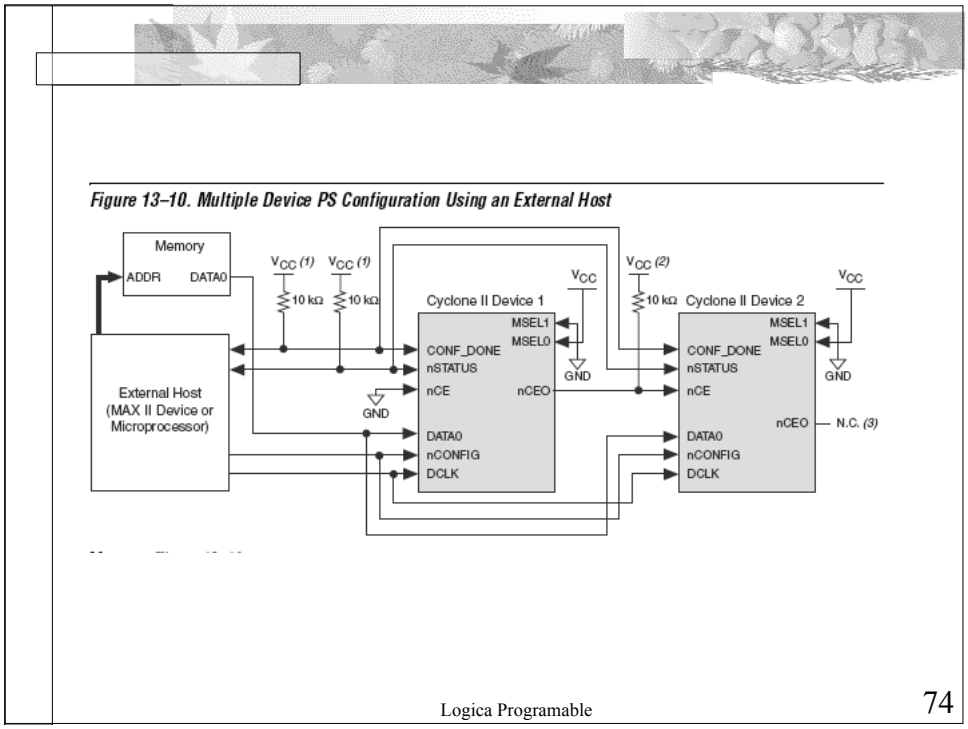
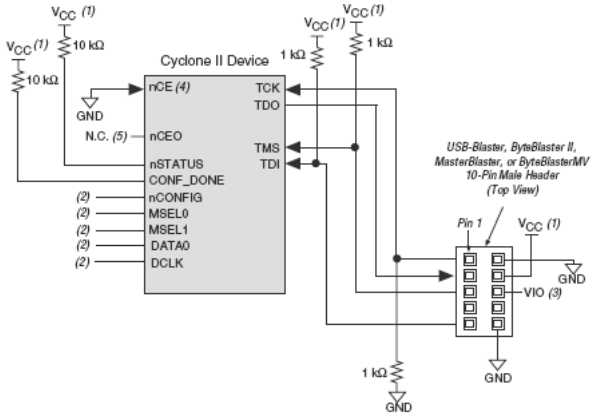
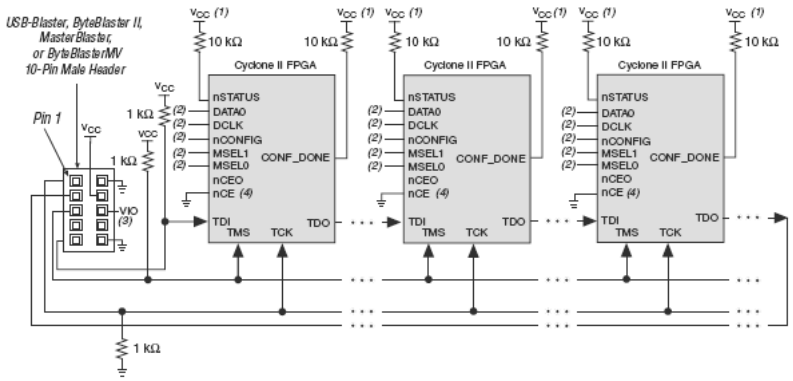
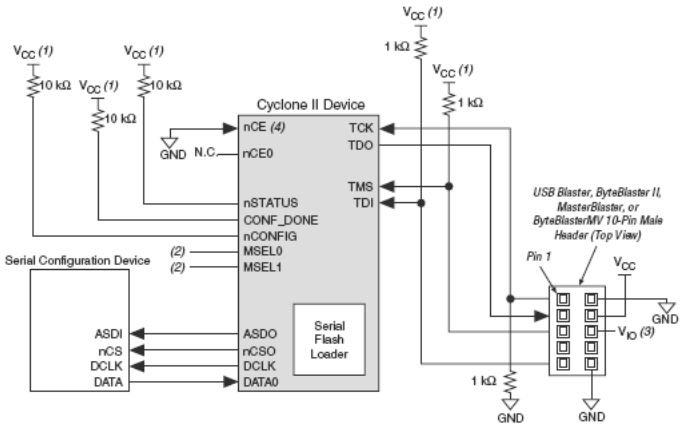


Figure 13–10. Multiple Device PS Configuration Using an External Host
Memory
ADDR
DATA0
External Host (MAX II Device or Microprocessor)
VCC (1)
VCC (1)
VCC (2)
10 kΩ
10 kΩ
10 kΩ
VCC
Cyclone II Device 1
Cyclone II Device 2
MSEL1
MSEL0
CONF_DONE
nSTATUS
nCE
nCEO
GND
DATA0
nCONFIG
DCLK
N.C. (3)
74

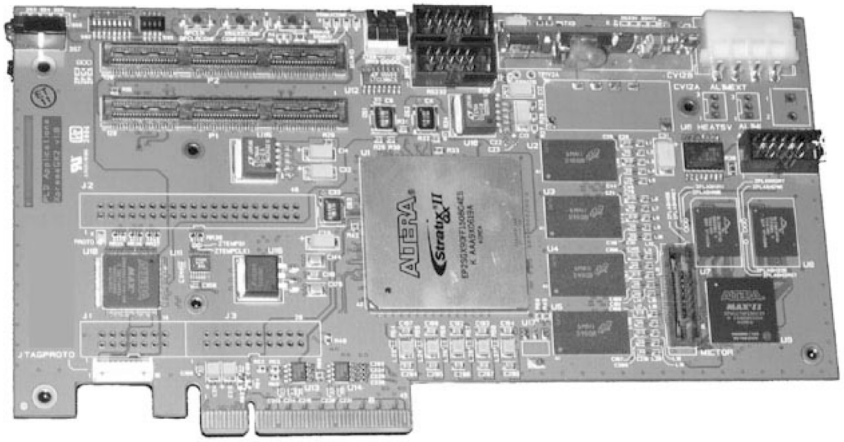
Figure 13–22. JTAG Configuration of a Single Device Using a Download Cable

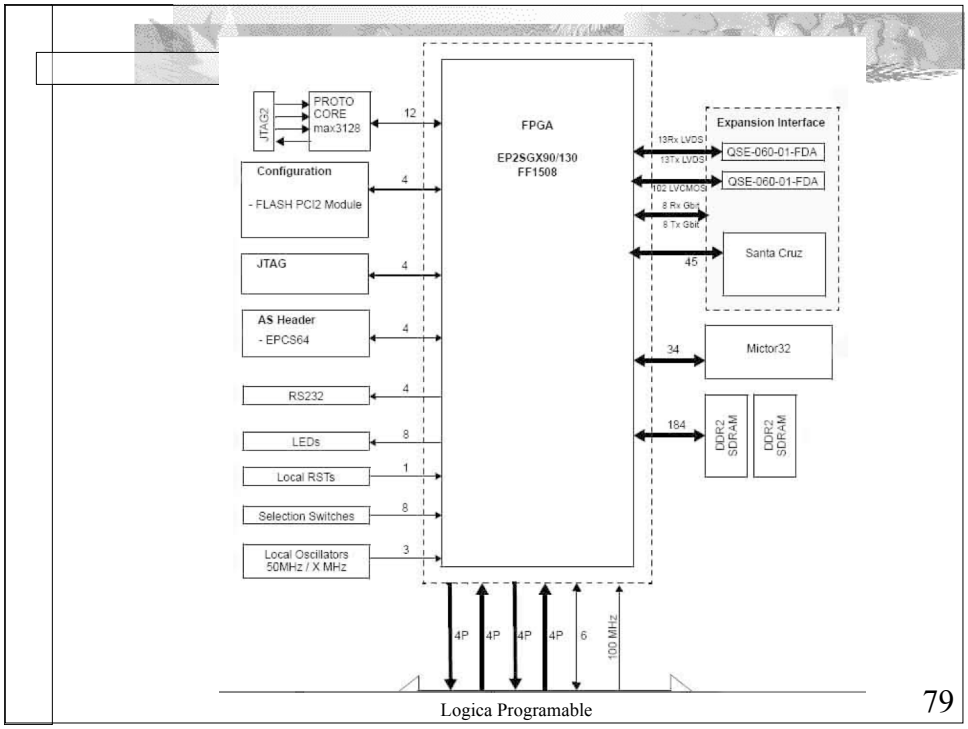


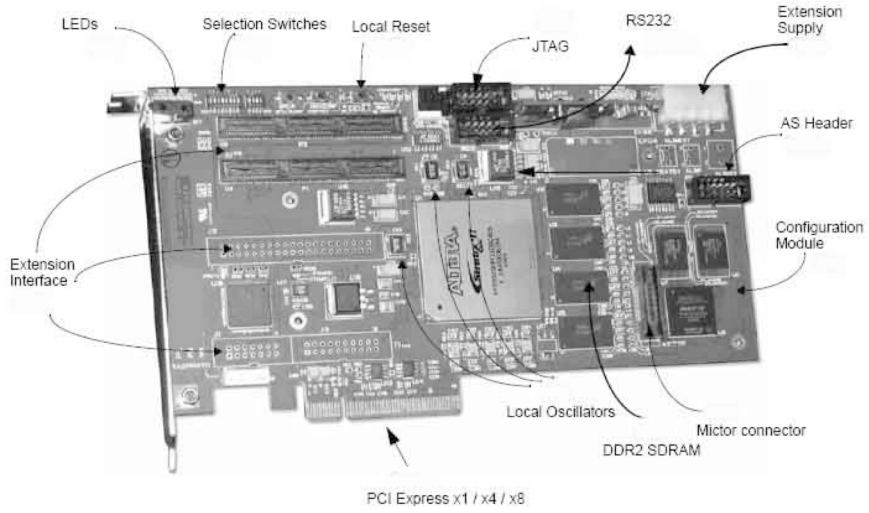




PCBs genéricas de desarrollo




JTAG2
PROTO
CORE
max3128
12
Configuration
- FLASH PCI2 Module
4
JTAG
4
AS Header
- EPCS64
4
RS232
4
LEDs
8
Local RSTs
1
Selection Switches
8
Local Oscillators
50MHz / X MHz
3
FPGA
EP2SGX90/130
FF1508
Expansion Interface
13Rx LVDS
13Tx LVDS
QSE-060-01-FDA
102 LVCMOS
QSE-060-01-FDA
8 Rx Gbit
8 Tx Gbit
45
Santa Cruz
34
Mictor32
184
DDR2 SDRAM
DDR2 SDRAM
4P
4P
4P
4P
6
100 MHz


LEDs
Selection Switches
Local Reset
JTAG
RS232
Extension Supply
AS Header
Configuration Module
Extension Interface
Local Oscillators
Mictor connector
DDR2 SDRAM
PCI Express x1 / x4 / x8